EE 209 Homework 6
CMOS Gates

Name: _____Solutions_____

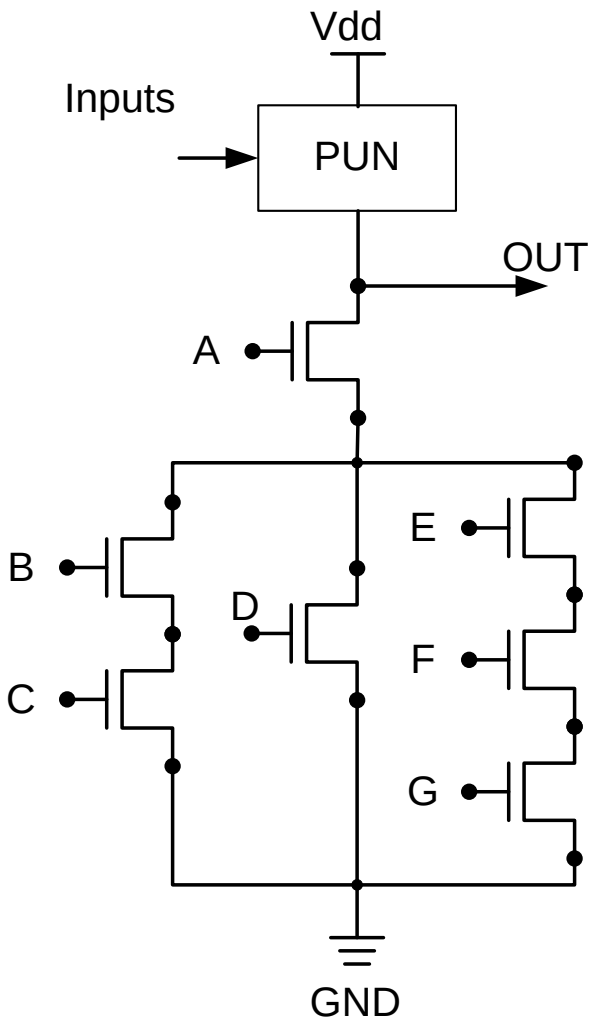
Due: See Website **Score: _____**

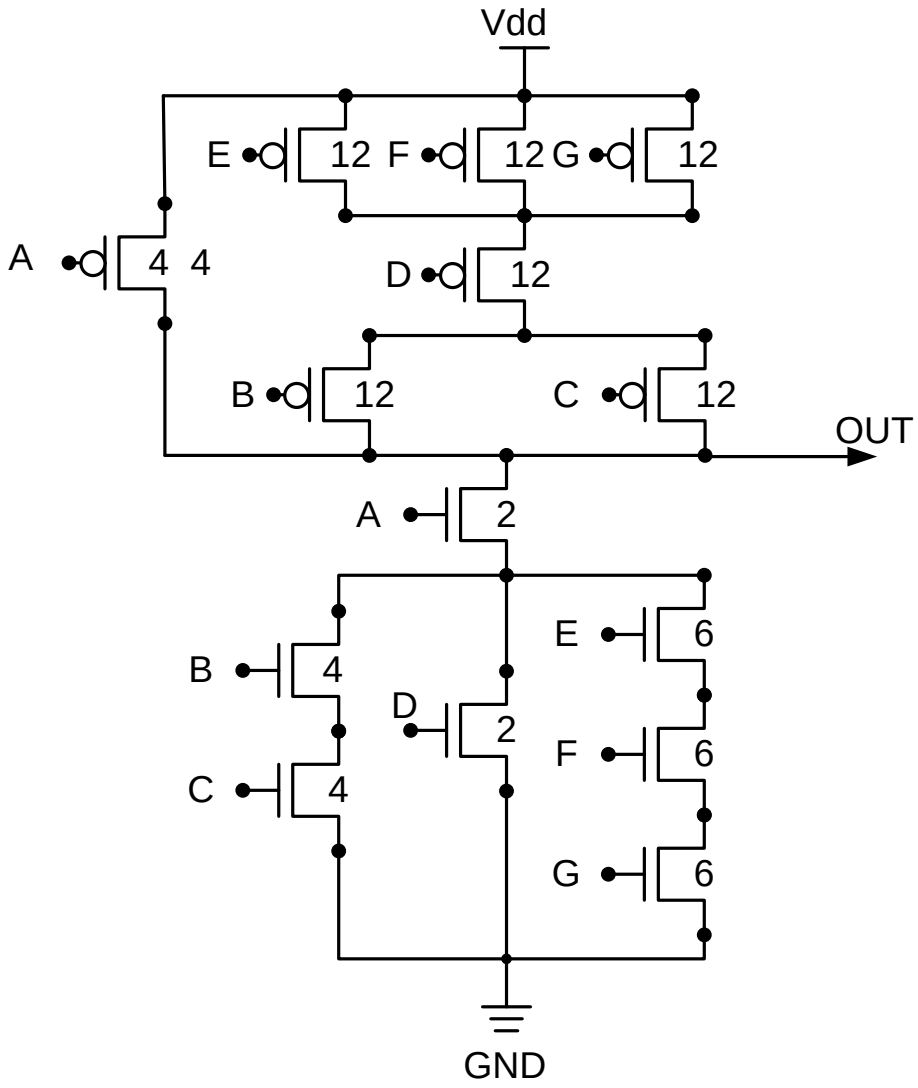
Paper Submission

[Helpful Videos to watch for your own knowledge]. Watch the following video clips on CMOS inverter fabrication and also the IC fabrication:

a. **CMOS Inverter fabrication: https://www.youtube.com/watch?v=OBiu2agne_U**
b. **An IC could have billions of transistors inside hundreds of millions of CMOS logic cells. The following video by Intel provides a very high level view of IC fabrication: https://www.youtube.com/watch?v=aCOyq4YzBtY**
c. **The following video is based on old technologies, however it still provides some useful information: https://www.youtube.com/watch?v=gBAKXvsaEiw**
d. **Interesting video on one application of PN junctions for solar cells. You can watch the video to see how solar energy can create electric power: https://www.youtube.com/watch?v=ZAxCvHxlLh8**

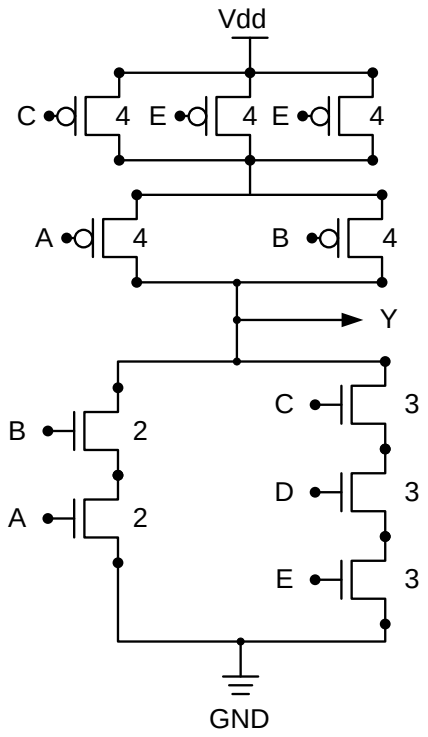
1. **Given the following pull-down for a CMOS compound gate.**
   a. **Draw the Pull-up network.**
   b. **Write the Boolean equation of OUT.**
   c. **Go back and show the widths of each NMOS and PMOS transistor such that the current in the worst case for rise time and fall time is equal to that of an inverter with minimum sized NMOS and equal rise and fall time.** $\mu_n/\mu_p = 4$.





OUT = [A•(BC + D + EFG)]'

2. **CMOS and Sizing**
   a. **Draw the transistor level diagram of Y = (AB + CDE)' using a CMOS approach. Assume the complements (inverse) of each input is NOT available. Try to minimize the number of transistors used.**
   b. **Annotate your transistor schematic design from problem 1 to show transistor widths (sizes) so that your implementation of Y matches the equivalent pull-up and pull-down resistance of a CMOS inverter. Assume the mobility ratio (i.e. μ_n/μ_p) is 2 and use minimum length transistors (L=1)**

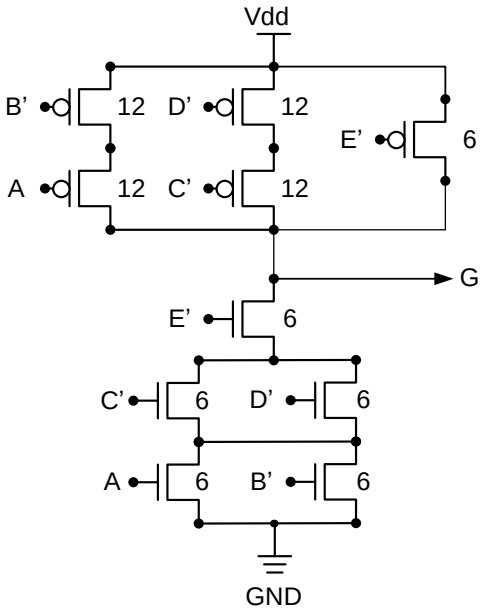


3. **CMOS and Sizing**

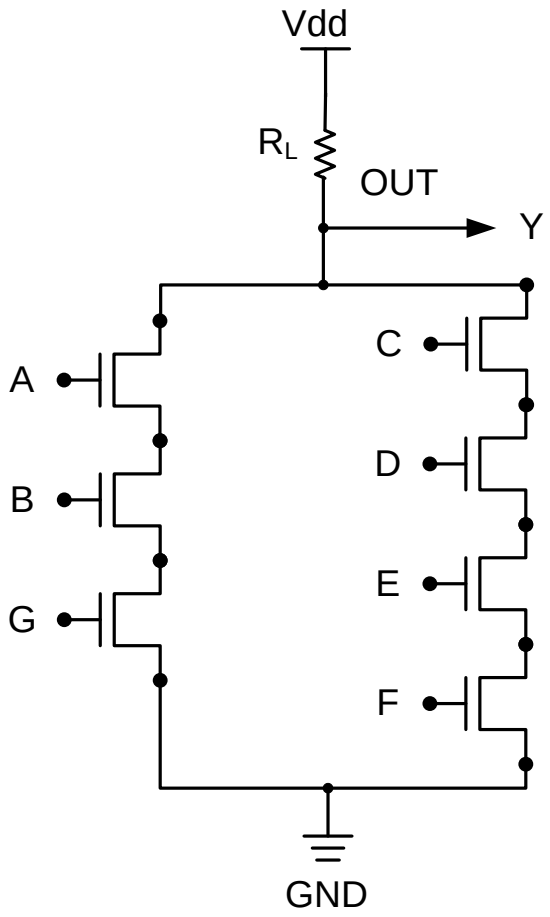
   a. **Design a CMOS circuit that implements $G = [A'B + CD + E]$. Size the transistors such that the CMOS circuit is twice as strong as a reference inverter with NMOS W=1 and PMOS W=3 size. (Assume inputs A, B, C, D and E as well as their complements are available).**

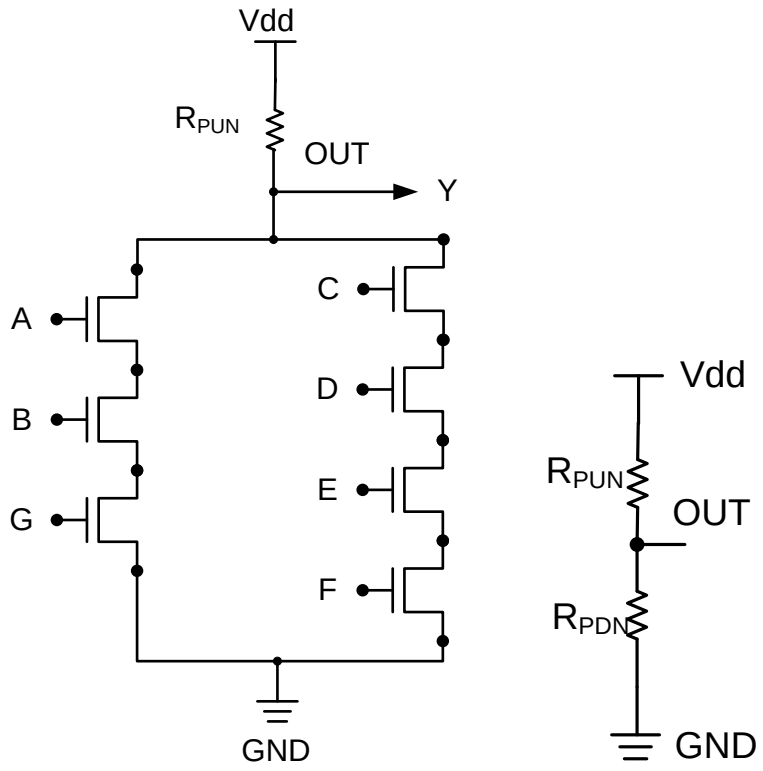
   Note: We want this circuit to be TWICE as strong as an inverter with NMOS W=1 and PMOS W=3, so we double everything.

$$G = \overline{\overline{[A'B + CD + E]}} = \overline{[(A + B')(C' + D')(E')]}$$



4. **NMOS-only and Resistive Loads**
    a. **Draw the schematic of Y = (ABG + CDEF)' using an NMOS-only approach (normal PDN using NMOS transistors but a single resistor in place of the PUN).**
    b. **Now, assuming that the input combination is such that the output *should* produce a logic '0' and that each NMOS transistor has a resistance of 5Kohm in linear mode, what value resistor would you be needed for the PUN to ensure Vout is at most 0.25*Vdd for the worst case input combination.**





If we model the PUN and PDN as single resistors we can use the voltage divider equation:
Vout = (R_{PDN} / (R_{PDN} + R_{PUN})Vdd

The worst case of RPDN is when it is larger since more voltage will be dropped across it. Thus the worst case is when C,D,E,F = 1,1,1,1 while A,B,G != 1,1,1. If each transistor is modeled as 5Kohms, then we have the equation.

0.25Vdd = (20K / (20K + R_{PUN}))Vdd
0.25 = (20K / (20K + R_{PUN}))
5K + 0.25R_{PUN} = 20K
0.25R_{PUN} = 15K
R_{PUN} = 60Kohms

5. **Prove that the unit of RC is seconds.**

I = Q (charge) / T (seconds)
R = V/I
C = Q / V
Thus RC = (V/I) * (Q/V) = Q/I = Q/(Q/T) = T

6. **RC Transient Analysis: Given the RC circuit on page 9 of unit 18, verify the formulae given on page 11 for the time constant, the propagation delay and the transition time (based on 10%VDD and 90%VDD crossing points) of the output voltage. Show the details of your work.**

Use the equation for when a capacitor is discharged and then at time = 0 a voltage source equal to Vdd is applied:

$$V_c(t) = V_{dd}\left[1 - e^{-\frac{t}{RC}}\right]$$

Time constant (i.e. Vc = 0.63Vdd when t = RC)

$$0.63 * V_{dd} = V_{dd}\left[1 - e^{-\frac{t}{RC}}\right]$$

$$0.37 = e^{-\frac{t}{RC}}$$

$$ln(0.37) = -\frac{t}{RC}$$

$$RC * -ln(0.37) = t \approx RC$$

Propagation delay

$$0.5 * V_{dd} = V_{dd}\left[1 - e^{-\frac{t}{RC}}\right]$$

$$ln(0.5) = -\frac{t}{RC}$$

$$t = 0.69 * RC$$

Transition time delay (10%-90%) = Time it takes to get to 90% - Time it took to get to 10%

Time it takes to get to 90%

$$0.9 * V_{dd} = V_{dd}\left[1 - e^{-\frac{t}{RC}}\right]$$

$$ln(0.1) = -\frac{t}{RC}$$

$$t = 2.3 * RC$$

Time it takes to get to 10%

$$0.1 * V_{dd} = V_{dd}\left[1 - e^{-\frac{t}{RC}}\right]$$

$$ln(0.9) = -\frac{t}{RC}$$

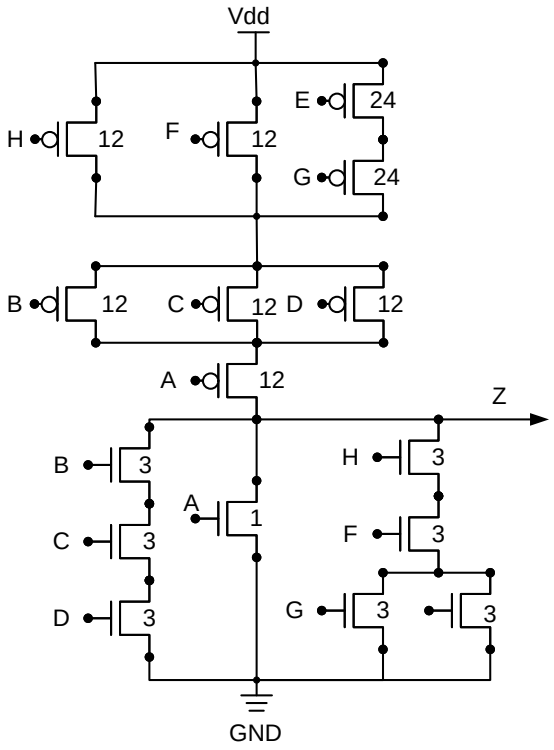
$$t = 0.1 * RC$$

Transition Time = 2.3RC – 0.1RC = 2.2RC

7. **Inverter Transient Analysis: The equivalent resistance values of a PMOS and an NMOS in an Inverter are 10KOhms and 7KOhms, respectively. The inverter drives an effective capacitance of 10fF (fF= femtoFarads = 10^{-15} Farads). Ignore other parasitic (internal) capacitances. Using an equivalent RC model to calculate the a.) propagation delay, b.) time constant and c.) transition time (based on 10%VDD and 90%VDD) for <u>BOTH</u> the rising output case and falling output case.**

	Rising	Falling
Prop. Delay (0.69RC)	0.69*Rp*C = 0.69*10K*10^{-15} = 6.9ps	0.69*Rn*C = 0.69*7K*10^{-15} = 4.83ps
Time Constant = RC	Rp*C = 10K*10^{-15} = 10ps	Rn*C = 7K*10^{-15} = 7ps
Transition Time (2.2RC)	2.2*Rp*C = 2.2*10K*10^{-15} = 22ps	2.2*Rn*C = 2.2*7K*10^{-15} = 15.4ps

8. **CMOS Logic Design and Transient Analysis:**
   Below is the CMOS logic cell that outputs Z = ~(A+BCD+HF(E+G)). The transistors are sized assuming a mobility ratio of 4.
   a. **The equivalent resistance of an NMOS with a size of 1W is measured as 10KOhms and for a PMOS of size 1W is 40KOhms. The effective capacitance of the load is approximated as 100fF. Ignore other parasitic (internal) capacitances. Calculate the propagation delay (time for output to reach 0.5Vdd) of falling output in the <u>WORST CASE</u> scenario. Repeat for the rising output.**
   b. **Repeat your calculations to now find the <u>BEST CASE</u> propagation delay of the falling output and rising output**



a.)
When the PDN is on we will see a ratio of W/L = 1 => 10KOhms
Prop. Delay (Falling) = 0.69*10Kohms*100E-15 = 0.69ns (690 ps)

When PUN is on, we will see W = 12 / L = 3 for a ratio of 4. Thus, since 1W/1L = 40Kohms, then W=12/L=3 => 10KOhms
Prop. Delay (Rising) = 0.69*10Kohms*100E-15 = 0.69ns (690 ps).

b.) The best case is when all transistors are on. (Recall that resistors in parallel yield Req = $(1/R1 + \ldots + 1/Rn)^{-1}$

If an NMOS with W/L =1 yields an equivalent 10Kohm resistance, then a W/L=3 NMOS transistor has resistance of 10K/3. When B,C,D are on in series we have 10K/3 + 10K/3 + 10K/3 = 10K. Transistor A is just 10Kohms and H,F,E,G yields (10K/3 + 10K/3 + (10K/6)). So we have a parallel connection of:
10K || 10K || 10K(5/6). = $(1/10K + 1/10K + 6/50K)^{-1}$ = $(16/50K)^{-1}$ => equivalent R_{PDN} = 50K/16

Thus fall time is 3.125K * 100E-15 = 312.5 ps

For the PUN the best case is when they are all on. Thus A is 40K/12. That is in series with 40K/(12*3) = 40K/36 for B,C,D. The same equivalent resistance (40K/36) is found for H, F, E and G. Putting these in series yield R_{PUN} = 40K/12 + 2*40K/36 = 50K/9 = 5.55Kohms

Thus rise time is 5.555 K * 100E-15 = 555.5 ps

9. **CMOS Inverter Static Analysis:**
   Setup a KCL equation to calculate the output voltage (Vout) of a CMOS inverter with sizes W and 2W (for the NMOS and PMOS, respectively) if the input is permanently connected to a high voltage of 2.4V. Assume VDD = 3.0V, Vtn = |Vtp| = 0.4V, $k_n=2k_p$. You need only setup the equation and manipulate it to be of the form 0 = $aV_{out}^2 + bV_{out} + c$. Hint: Use an educated guess for the approximate level of V_{out} to determine the mode of operation of each transistor.

   First, recognize both transistors are on: Vgs,n > Vtn (2.4 > 0.4) and Vgs,p < Vtp (-0.6 < -0.4). So to find what mode each transistor is operating we need to "know" Vds,n and Vds,p. Since this is an inverter and the input is "high-ish" the output should be "low-ish". If that is the case then V_{out} is small. Note that Vds,n = Vout and Vds,p = Vdd-Vout. So if the output is low-ish we should see that Vgs,n-Vtn > Vds,n and thus the NMOS is in LINEAR. For the PMOS, |Vds,p| > |Vgs,p|-|Vtp| and thus it is in SATURATION mode. From here we can setup our KCL equation since the current through the PMOS must be the same as through the NMOS.

   Ipmos = Inmos
   $0.5*kp*2W*[0.2]^2 = 0.5*kn*1W*[2*2.0V*Vout – Vout^2]$ =

   $0.5*kp*2W*[0.2]^2 = 0.5*2*kp*1W*[4.0V*Vout – Vout^2]$ =

   $0.04 = [4.0V*Vout – Vout^2]$

   $1 = [4.0V*Vout – Vout^2]/0.04$

   $0 = -25*Vout^2 + 100*Vout - 1$