OBJECTIVE

Investigate the potential benefits of power saving by using extreme dynamic voltage scaling for QDI design.

• No clock-related issues.
• Robust towards PVT variations.
• Scaling down the supply voltage is not risky.
• Error recovery cost is avoided.

16X16 Dual-Rail QDI MAC Unit

QDI Multiplier

QDI Adder

Tools & Technology

Synopsys Tools: Design Vision & IC Compiler.
Cadence: Virtuoso.
Global Foundry GF 65nm 12mm.
ARM Standard Cells.

Fabricated Chip

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