EE 457 Homework 7

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Name: _____ Score: _____/ 100_

Virtual Memory

Reproduced below is Figure 5.32 (page 443) of the 5th Ed. of your textbook.

Option	TLB	Page Table	Cache	Possible? If so, under what circumstances
1	Hit	Hit	Miss	Possible, although the page table is never really checked if TLB hits
2	Miss	Hit	Hit	TLB misses, but entry found in page table; after retry, data is found in cache
3	Miss	Hit	Miss	TLB misses, but entry found in page table; after retry, data misses in cache
4	Miss	Miss	Miss	TLB misses, and is followed by page fault; after retry, data must miss in cache
5	Hit	Miss	Miss	Impossible: cannot have a translation in TLB if page is not present in memory
6	Hit	Miss	Hit	Impossible: cannot have a translation in TLB if page is not present in memory
7	Miss	Miss	Hit	Impossible: data cannot be allowed in cache if the page is not in memory

1.) [15 pts.] Answer the questions below using the table above.

a.) (4 pts.) Based on the **bottom three rows** of the above table, we can say that if the page is _____ (**present / absent)** in the main memory, then there _____ (**will be / can't be)** a _____ (**hit / miss)** in _____ (**TLB / Cache / either TLB or Cache / neither TLB nor Cache).**

b.) (1 pts.) By **increasing the main memory size**, we can be sure to increase the HIT rate of _____ (**Cache / TLB / PT**).

c.) (5 pts.) Consider the 1st row of the table above. While a _____ (**hit / miss**) in the TLB guarantees a _____ (**hit / miss)** in the page table, we note that a _____ (**hit / miss)** in the TLB _____ (**does / does not)** necessarily imply _____ (**either a hit or a miss / neither a hit nor a miss)** in the page table.

d.) (2 pts.) Before a page in the main memory is removed (and perhaps copied back to the secondary storage), any blocks of the page in the _____ (**cache / TLB)** are to be flushed to the main memory and the corresponding translation entry in TLB shall be _____ (**validated / invalidated).**

e.) (1 pt.) Replace of an entry in the TLB is _____ (**possible even though / impossible if)** no pages are altered in the main memory (i.e. no new page is brought into the main memory or no existing page has been removed from main memory).

f.) (1 pt.) Replace of a block in cache is _____ (**possible even though / impossible if)** no pages are altered in the main memory (i.e. no new page is brought into the main memory or no existing page has been removed from main memory).

g.) (1 pt.) The block in cache that is being replaced or removed (circle one):

i. Is never written back to the main memory.
ii. Is always written back to the main memory.
iii. Written back to the main memory if write-back policy is used and the block is modified during its residency in the cache.

2.) [30 pts.] Consider Figure 5.30 (441) from the 5th Ed. of your textbook and then answer the questions.

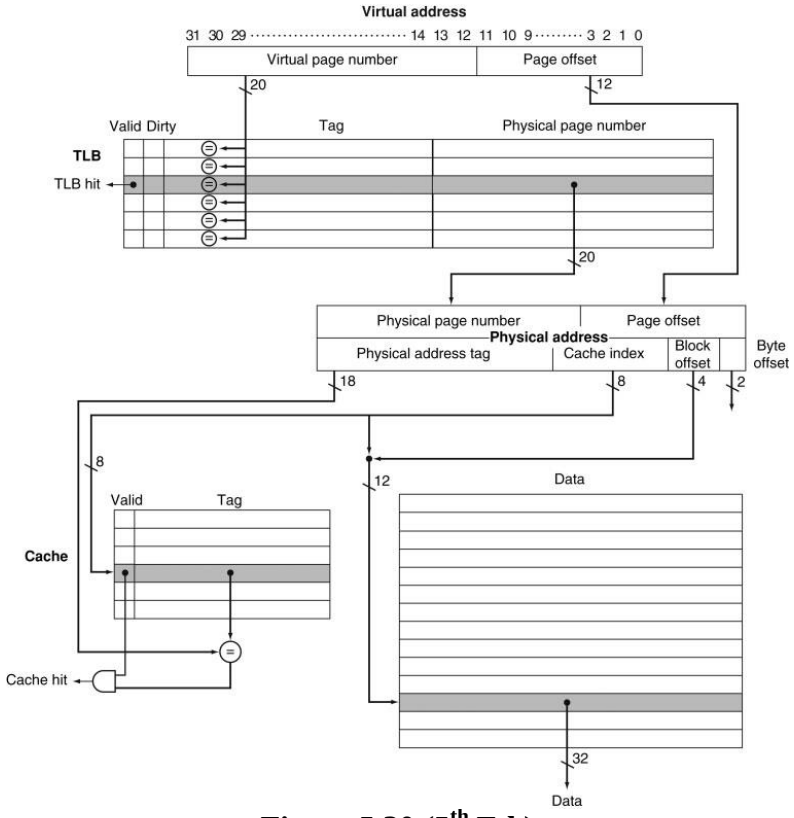

Figure 5.30 (5th Ed.)

a.) (3 pts.) From this figure we can tell that the TLB uses _____
(**fully associative mapping / set-associative mapping / direct-mapping**) because:
_____
_____
_____
_____
_____

b.) (3 pts.) From this figure we can tell that the cache uses _____
(**fully associative mapping / set-associative mapping / direct-mapping**) because:
_____
_____
_____
_____
_____

c.) (2 pts.) To search for an entry in the TLB we need _____
(**1 comparator / 2 comparators / as many comparators as entries in the TLB**) and each comparator is of _____-bits (in width).

d.) (2 pts.) The design in this figure uses _____
(**Physical address tag / Cache index / Block offset / a concatenations of...)** to index the TAG RAM of the data cache.

e.) (2 pts.) The design in this figure uses _____
(**Physical address tag / Cache index / Block offset / a concatenations of…**) to index the data cache data RAM.

f.) (2 pts.) The shaded area in the cache data RAM is _____
(**an entire block / only a part of a block**).

g.) (2 pts.) The size of a data cache block is _____ bytes. This information is obtained from looking at the size of the _____ (state the name of the field(s)).

h.) (4 pts.) We _____ (**have to / don't have to**) wait until the translation from virtual address to physical address is done to access the cache. This architecture is called _____ (**physical indexed physically tagged (PIPT) / virtually indexed physically tagged (VIPT)**) cache.

i.) (6 pts.) To convert the current scheme to the other (PIPT to VIPT or VIPT to PIPT as the case may be), we can perhaps: i) consider _____ (**increasing / decreasing**) the page size to _____ Kbytes from the current size of _____ Kbytes, or ii) consider _____ (**increasing / decreasing**) the cache size to _____ Kbytes from the current size of _____ Kbytes.

j.) (2 pts.) Usually the TAG RAM is different and separate from Data RAM in cache. However, in some cases the TAG RAM and the Data RAM can be combined into one wide RAM if the _____ (**depth / width**) is the same for both TAG and DATA RAM.

k.) (2 pts.) The size of a data cache block is _____ bytes. This information is obtained from looking at the size of the _____ (state the name of the field(s)).

3.) (10 pts.) The bits of a tag taken from part of the virtual page number of a virtual address may be present in (choose all that apply)

i. A TLB.
ii. The 1st level (page directory) of a 2-level page table.
iii. The 2nd level (page table) of a 2-level page table.
iv. Main memory
v. Tag of the data cache (PIPT)
vi. Data memory of the data cache

Explain your answer:

_____

_____

_____

_____

4.) [27 pts.] Consider the following parameters for a system with 24-bit address / 32-bit data CPU.

Page Size	2 KB (2^{11})
TLB Size	32-entry (2^5)
TLB Organization	2-way set associative
Cache Size	256KB (2^{18})
Block Size	Two 32-bit words
Set Size	4 blocks per set

Assume that the virtual address 0x345678 maps to the physical address 0xBA9E78. Also assume that when the processor tried to read the 32-bit word at the virtual location 0x345678, there was a hit in TLB and a hit in the data cache as well.

a.) (6 pts.) Write down the virtual address 0x345678 in binary and show its division into page-offset and virtual page number fields. Further show the division of the virtual page number into set and tag fields based on the TLB parameters provided above.

Address bits to complete in binary and then indicate the divisions.

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	/BE[3:0]

b.) (2 pts.) If the sixteen sets in the TLB are numbered in binary from 0000-1111, which set was chosen?

c.) (4 pts.) How many comparisons and of what size (include the valid bit) were performed to see if the translation was available in the TLB?

d.) (3 pts.) How sets does the 256KB data cache consist of? _____

e.) (6 pts.) Write down the physical address 0xBA9E78 in binary and mark the word, set, and tag fields based on the data cache parameters provided above.

Address bits to complete in binary and then indicate the divisions.

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	/BE[3:0]

f.) (1 pts.) Which set did the cache controller choose (index)? _____

g.) (4 pts.) How many comparisons and of what size (include the valid bit) were performed to see if the block was available in the cache?

h.) (1 pts.) If you wish to have "wide" memory to facilitate fast moving of a block from the main memory to the cache in a single transfer. How wide to you wish to organize main memory? _____ (**256- / 128- / 64- / 32- / 16- / 8-**) bits.

5.) [18 pts.] Consider the following 32-bit virtual address, 32-bit physical address, 16-bit data (1 word = 16-bits) byte addressable system using little endian word ordering. In the place of A0 we have /BE1 and /BE0 to select odd / even byte access (respectively). Use the terms VA31-VA1 (virtual address), PA31-PA1 (physical address), /BE1, /BE0 in your answers below.

Page Size	32 KB (2^{15})
TLB Size	128-entry (2^{7})
TLB Organization	2-way set associative
Page Table Org.	2-level. Level 1 (Page Directory) = 1024 (2^{10}) entries followed by appropriate level 2 tables.
Cache Size	128KB (2^{17})
Block Size	Two 16-bit words
Set Size	4 blocks per set

a.) (2 pts.) The VPN is broken into _____ bits for the VPN and ____ bits for the page offset.

b.) (4 pts.) To facilitate fast lookup the TLB is broken into _____ RAMs. Each RAM stores the virtual tag (for comparison) + a valid bit + the actual physical page number (PPFN). This means the TLB RAM sizes are each (_____ x ___). To index/address each TLB RAM we use what bits of the VA: _____.

c.) (1 pts.) To check for a hit in the TLB we require 2 comparators of width _____ (including the valid bit).

d.) (4 pts.) If the TLB misses, we must access the page table to attempt to find a translation. To index the first level of the page table (i.e. the page directory) we would use what bits of the VA: _____. We would further use what bits of the VA to index the 2nd level of the page table: _____.

e.) (1 pts.) The _____ (**1st level / 2nd level / both**) page table(s) contains translations (i.e. PPFNs).

f.) (1 pts.) The width of a PPFN is _____-bits.

g.) (4 pts.) The data cache consists of _____ (how many) TAG RAMs of size _____x____ (include the valid bit) and we would use which bits of the PA to index these TAG RAMS: _____?

h.) (2 pts.) Upon a data cache hit we would use which bits of the PA to index/address the DATA RAMs? _____

