# EE457: Computer Systems Organization
Select Problems from Summer 2020 Final

1. **(14 pts.) OOO Execution**:   Given the OoO execution, In-order completion processor below with separate Integer ALU/Branch unit, Mul/Div unit, and Load/Store unit, each with **2 reservation stations (2-slot issue queues)** and an ROB with **7 locations**, consider the code below, identify data dependencies, and indicate the status of each instruction when the **indicated cache miss resolves (i.e. is complete) assuming a cache miss requires 100 cycles to complete**. While not necessary, you can assume 1 instruction is issued every cycle and 1 can be committed every cycle, and that each execution unit takes 1 cycle to compute.
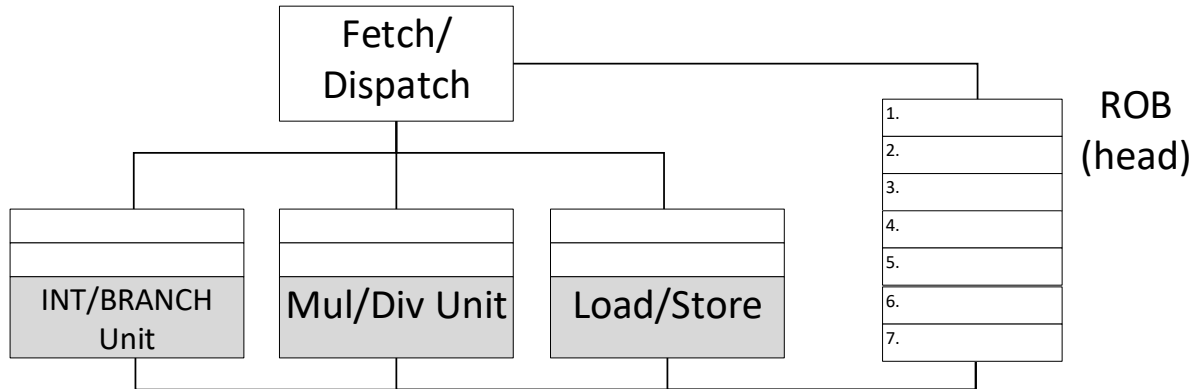
For each instruction, first indicate what previous instruction(s), if any, it directly depends upon for data. Use '-' if the instruction is independent. Then place an **X in the column** that describes the status of the instruction **when the cache miss completes**.. (only 1 X per row…the options are mutually exlusive)

Num	Instruction	Depends On [Instruc. Num(s) or –]	Committed and Left the ROB	Completed and waiting in the ROB to Commit.	Waiting to Execute	Not yet dispatched
1	add $2, $3, $4	-				
2	or $5, $6, $7					
3	lw $3, 0($2) **# cache miss**					
4	sub $8, $2, $5					
5.	and $9, $3, $7					
6	mul $10, $9, $7					
7	div $11, $2, $4					
8	sw $8, 0($5) **# cache hit**					
9	mul $12, $10, $5					
10	add $13, $9, $4					
11	or $14, $6, $7					
12	lw $5, 4($2) **# cache hit**					
13	div $15, $9, $2					
14	and $16, $6, $7					

2. **(15 pts.) Caching.** Suppose you are given a system with 16-bit address and the following bits are used to access a **direct-mapped** cache.

Address Bits	15-10	9-5	4-2	1-0
Field	Tag	Index	Word offset	Byte enables

a. How many bytes total is the cache data memory? _____

b. How large is the tag RAM (rows x columns): _____ x _____ (include V bit, but not Dirty bit)

c. Examine the following address trace/sequence and indicate which will result in a hit or miss. Also indicate if a block will be evicted by an access.

Decimal Address	Equivalent Binary Address	Hit/Miss (Circle your answer)	Causes Eviction (Circle if Yes)
0	0000 0000 0000 0000	Hit / Miss	Yes
4	0000 0000 0000 0100	Hit / Miss	Yes
16	0000 0000 0001 0000	Hit / Miss	Yes
132	0000 0000 1000 0100	Hit / Miss	Yes
232	0000 0000 1110 1000	Hit / Miss	Yes
160	0000 0000 1010 0000	Hit / Miss	Yes
1024	0000 0100 0000 0000	Hit / Miss	Yes
30	0000 0000 0001 1110	Hit / Miss	Yes
140	0000 0000 1000 1100	Hit / Miss	Yes
3100	0000 1100 0001 1100	Hit / Miss	Yes
180	0000 0000 1011 0100	Hit / Miss	Yes
2180	0000 1000 1000 0100	Hit / Miss	Yes

3. **(15 pts.) MESI Cache Coherence Protocol:** Examine the table below showing sequence of memory accesses performed by three processors in a shared memory multiprocessor. Assume all caches are empty initially. Assume cache blocks of a single word (so we only show 1 data value). Show what bus requests and responses are initiated and the state of the block after each operation as well as what data is in memory.

(Bus Requests/ACtions: **BusRd**=Read, **BusRdX**=Read w/ Intent to Write, **BusUpgr** = Invalidate5others, **Flush** = Supply data on bus)

Memory Access	Bus Request / Response	P1 Cache State {M,E,S,I}	P2 Cache State {M,E,S,I}	P3 Cache State {M,E,S,I}	Mem. Data @ address X
P1 Write X=5					4
P1 Read X					
P2 Read X					
P1 Read X					
P2 Write X=6					
P3 Read X					
P2 Read X					