Su. '16 Syllabus **EE 457** Redekopp

Computer Systems Organization

Abstract:
This course covers computer organization and design. It provides CS/CE/EE students a substantial understanding of a CPU at its logic design level. Design of the control unit and the data path unit of a simple multi-clock-cycle CPU and a pipelined CPU is covered in detail. Hardware support for exceptions, dynamic scheduling of instructions (Tomasulo algorithm to execute instructions in an out-of-order fashion), and branch prediction are also discussed. Computer arithmetic and memory hierarchies (cache, main memory, virtual memory) are also covered. Hardware-software interface is discussed. Students design in Verilog and use ModelSim simulator to verify their design/simulation exercises.

At the end of the course, students are expected to feel confident to perform logic design of CPU structures or other hardware systems utilizing pipelining and other RTL techniques and proceed to graduate courses in computer architecture or general hardware design.

Instructor Info:

Instructor:	Mark Redekopp	Office Hours:	T,Th: 8:00-9:00 (1st 3 weeks)
Office:	EEB 222		T,Th: 11-12 (2nd 3 weeks)
			W: 10-12 (all 6 weeks)
E-mail:	redekopp@usc.edu	Office Phone:	(213) 740-6006

TA and Grader Info:

TA:	Pezhman Mamdouh	Grader	TBA
Office:	See website	Office:	See website
Office Hours:	See website	Office Hours:	See website
E-mail:	mamdouh@usc.edu	E-mail:	See website

Course Materials and Info:

URL (Blackboard):	http://bits.usc.edu/ee457 https://courses.uscden.net/d2l/home
Textbook (Required):	Patterson and Hennessy, "Computer Organization and Design: The Hardware/Software Interface", 5th ed. (ISBN: 978-0-12-407726-3)
Course Notes:	Available from the bookstore

Grading Policy:

Homework =	15%
Labs =	20%
1 Midterm =	30%
Final Exam =	35%

Homeworks: *Homeworks are designed to prepare you for the problems and skills you will need for the exams*. They will also be representative of the style of problems you will see on exams. *It is expected that each student will present their own work in their own creative way. (You should show all work/steps used to arrive at the solution)*. Copying or allowing others to copy homeworks will result in a 1 letter grade deduction for the **entire course**. Homeworks should be done **neatly and be stapled together**. Homeworks are due **at the beginning (of before, if DEN)** of **lecture**. Late assignments will be accepted for 2 days after the due date with a 20% deduction per day. Solutions will be posted 2 days after the due date after which no late work will be accepted unless accompanied by a valid excuse. If you have extenuating circumstances, e-mail me so we can work out an arrangement.

Labs: Labs are critical not only to your grade but are really the true evaluation of your learning. The labs in this class are intended to prepare you with the skills needed to succeed in industry and real-world jobs. Copying or allowing others to copy labs will be reported to SJACS and will likely lead to an F in the course. Labs are to be turned in to your **discussion** leader. Late assignments will be accepted for 2 days after the due date with a 20% deduction per day. After 2 days it will not be accepted. If you have extenuating circumstances, e-mail me so we can work out an arrangement.

Exams: All exams will be closed book. There will be no calculators allowed, just bring a few pencils and an eraser. Any cheating will result in an "F" in the course and will be referred to Student Affairs for other penalties. Make up exams will only be given for valid medical or family emergency excuses (proof required).

Attendance: You are expected to attend ALL lectures. Missing more than 1 class may result in deductions in your participation grade.

Academic Integrity: The use of unauthorized material, communication with fellow students during an examination, attempting to benefit from the work of another student, and similar behavior that defeats the intent of an examination or other class work is unacceptable to the University. It is often difficult to distinguish between a culpable act and inadvertent behavior resulting from the nervous tension accompanying examinations. When the instructor determines a violation has occurred, appropriate action, as determined by the instructor, will be taken. All students should read, understand and abide by the University Student Conduct Code http://www.usc.edu/dept/publications/SCAMPUS/governance/gov03.html

Academic Accommodations: Any student requiring academic accommodations based on a disability is required to register with Disability Services and Programs (DSP) each semester. A letter of verification for approved accommodations can be obtained from DSP. Please be sure the letter is delivered to me as early in the semester as possible. DSP is located in STU 301 and is open 8:30 a.m. - 5:00 p.m., Monday through Friday. The phone number for DSP is (213) 740-0776.

Expectations: Attend class, do your assignments, ask questions and participate!

Course Schedule and Lecture Topics:

Wk	Mon.	Wed.	Textbook Sec.	Tentative Labs
7/5, 7/7	Class Overview Datapath Design Review **HW1 Out**	Control Unit Design	Ch. 1	Lab 1
7/12, 714	Fixed Point Arithmetic Fast Adders **HW 2 Out**	Instruction Sets MIPS ISA **HW3 Out**	Ch. 3.1-3.3 Ch. 2	Lab 2
7/19, 7/21	Performance Metrics Single Cycle CPU **HW 4 Out**	Single-Cycle CPU Pipelined Processor Design **HW 5 Out**	Ch. 1.4	Lab 3a
7/26, 7/28	Data Hazards Control Hazards	**Midterm** Cache Memory **HW 6 Out**	Ch. 4.1-4.3 Ch. 4.4-4.8 Ch. 4.9 Ch. 5.1	Lab 3b
8/2 8/4	Main Memory Organization Virtual Memory Exceptions **HW 7 Out**	Out-of-Order Execution Tomasulo Algorithm Branch Prediction Speculative Execution	Ch. 5.2-5.4 4.10 Class Notes 7.1-7.6	Lab 4a/b
8/9 8/11	Thread Level Parallelism Cache Coherency	**Final**	5.8 7.7, App. A	