EE 209
Fundamentals to Digital System Design
(4 Units)

Abstract:
This course introduces digital system design theory and practice. Focus is placed on logic design techniques and physical implementation methodologies. Utilizing the structures and concepts learned in EE 109, students will learn to design and synthesize combinational and sequential logic structures at the gate and transistor level. Topics include Boolean algebra, common datapath components, state machine synthesis, various implementation technologies with focus on CMOS, and physical layout. A lab component will familiarize students with common electronic design automation (EDA) software tools (mainly using FPGAs) and allow students to put theory into practice.

Learning Objectives: Upon completion of this course students will be able to:
1. Identify and derive appropriate logic functions to implement a specified design
2. Synthesize logic circuits to implement a given logic function
3. Understand design tradeoffs that include area and speed and optimize circuits for desired performance
4. Analyze and manipulate logic circuits to ascertain their logic function or alter their implementation based on specific design requirements
5. Synthesize and analyze circuits that include state elements (flip-flops) [i.e. state machines]
6. Design datapath and control units for portions of a simple CPU
7. Understand basic principles of semiconductor physics and transistor operation
8. Layout simple logic cells
9. Understand the relationship of delay and area due to the parasitics inherent in physical implementation.

Prerequisites: EE 109L

Instructor Info:

Instructor:	Mark Redekopp	Office Hours:	M: 11-12, 1-2:30 W: 11-12
Office:	EEB 222		Th: 1-1:40 F: 1-3
E-mail:	redekopp@usc.edu	Office Phone:	(213) 740-6006

TA's and Grader Info: See course website

Course Materials and Info:

Online Content (Blackboard):	**Content**: http://bits.usc.edu/ee209 **Grades & HW entry:** http://blackboard.usc.edu
Textbook (Required):	Frank Vahid, "Digital Design With RTL Design, VHDL, and Verilog, 2nd Ed.", John Wiley and Sons, 2011 (ISBN: 978-0470531082)
Textbook (Reference):	Kang and Leblebici. "CMOS Digital Integrated Circuits, 3rd Ed." McGraw-Hill, 2003.

Grading Policy:

Participation and Homework	10% (lowest HW thrown out)
Design Labs	25%
Midterm 1	30%
Final	35%

Homeworks: *Homeworks are your key to learning*. Only by doing problems on your own will you develop the logic skills and understanding to perform well on exams. You are expected to *present your own work with your own creative solutions.* **Experience has shown that those students who put in the effort on these homeworks, struggled with problems, asking questions when they did not understand a problem, did the best in this course.**

Homework should be submitted (usually via Blackboard) by the date posted on Blackboard. Any hard copy submissions should be neatly printed and be **stapled** together. If not due on Blackboard, a hard copy submission is due at the **beginning** of class. All circuit drawings should be neatly in Xilinx. **Late homework will be accepted with a 25% deduction per day** and should be slipped under my office door (or done on line via Blackboard). **Homework will not be accepted after solutions are posted** (2 days after the due date.) If you cannot make it to a lecture, turn it in early or have a friend turn it in. You will be expected to have read the listed sections of the textbook before each lecture.

Design Labs: We will primarily use Xilinx CAD tools to provide an opportunity to work with actual hardware and provide concrete examples to the pencil and paper designs discussed in lecture. FPGA boards will be available in lab and during TA office hours. Labs must be checked off at the **beginning of your discussion section** and submitted online as well immediately after being demoed. For late submission you must demonstrate and submit your code by the next scheduled TA office hours following the due date. Labs should be done. You should not show or share your code NOR look at anyone else's code. The penalty for similar code as a result of collaboration will be the loss of 2 full lab scores (i.e. 0 on two labs).

Exams: All exams will be closed book. We will utilize the Quiz Section for these exams. There will be no calculators allowed, just bring a few pencils and an eraser. You must show how you arrived at your answers to receive full credit. Any cheating will be referred to Student Affairs for appropriate action. Make up exams will only be given for valid medical or family emergency excuses (proof required).

Expectations: Attend lectures, do your homework, BE CURIOUS!

Academic Accommodations: Any student requiring academic accommodations based on a disability is required to register with Disability Services and Programs (DSP) each semester. A letter of verification for approved accommodations can be obtained from DSP. Please be sure the letter is delivered to me as early in the semester as possible. DSP is located in STU 301 and is open 8:30 a.m. - 5:00 p.m., Monday through Friday. The phone number for DSP is (213) 740-0776.

Statement on Academic Integrity
USC seeks to maintain an optimal learning environment. General principles of academic honesty include the concept of respect for the intellectual property of others, the expectation that individual work will be submitted unless otherwise allowed by an instructor, and the obligations both to protect one's own academic work from misuse by others as well as to avoid using another's work as one's own. All students are expected to understand and abide by these principles. *Scampus,* the Student Guidebook, contains the Student Conduct Code in Section 11.00, while the recommended sanctions are located in Appendix A: http://www.usc.edu/dept/publications/SCAMPUS/gov/. Students will be referred to the Office of Student Judicial Affairs and Community Standards for further review, should there be any suspicion of academic dishonesty. The Review process can be found at: http://www.usc.edu/student-affairs/SJACS/.

Emergency Preparedness/Course Continuity in a Crisis
In case of a declared emergency if travel to campus is not feasible, USC executive leadership will announce an electronic way for instructors to teach students in their residence halls or homes using a combination of Blackboard, teleconferencing, and other technologies.

Lecture and Assignment Schedule for EE 209:

A tentative schedule is posted on our website: http://bytes.usc.edu/ee209

Important Dates:

- **Midterm 1: Feb 22nd 7 p.m.**
- **Final: Tues May 8th at 8 a.m.**