EE 101 Homework 2
Redekopp

Name: ________________________________  Score: ________
Due: See Blackboard  [BB] = Blackboard Submission. For non-BB problems, show work to get full credit.

HW 2a Blackboard Form
1. [BB] Derive the truth table for the following functions by plugging in combinations to the equations below. Then use the truth table to write the algebraic representation of the minterm or maxterm expression (as indicated) for the function. (24 pts.)
   a. \[ F = (A' + B')(C) \]  [minterms only]
   b. \[ G = WX' + XY' + W' \]  [maxterms only]

2. [BB] Write out the algebraic form of both the minterm and maxterm representation for each function (both for each one…meaning convert G to a canonical product as well.) (10 pts)
   a. \[ G = \Sigma_{A,B,C,D} (2,3,6,13,15) \]

3. [Practice: Do not turn in or submit…check with solutions] Draw a schematic representation using logic gates (AND, OR, NOT) for the following Boolean equations (use bubbles at the inputs or outputs of AND and OR gates rather than drawing individual inverters)
   a. \[ F = X + ((W'Y'Z)(W+(X'(Y+Z)))) \]
   b. \[ G = AB+(D(B'+C)(A'+C)) \]

4. [BB] When the circuit below was fabricated on a chip, a problem occurred. One of the first level OR gates continually outputs a ‘1’ (a.k.a. a “stuck-at-1” fault) no matter what the inputs to the gate. (18 pts.)
   a. Propose and list a minimal number of input combinations that could be used to determine which gate had the fault (i.e. a,b,c = 1,1,0 and a,b,c = 1,1,1)? Describe how you could use these values to determine the gate with the error?
   b. If instead one of the OR gates was stuck at ‘0’ would any set of input combinations be able to determine which gate had the error? Explain?
HW 2b Blackboard Form

5. [BB] Convert each of the equations in question 3 to an equivalent 2-level implementation by distributing using T8/T8’ to get SOP or POS form. Simplify wherever possible to find the smallest SOP/POS expression. (12 pts.)
   a. \( F = X + [(W'Y'Z)(W+(X'(Y+Z)))] \) convert to POS
   b. \( G = AB + (D(B'+C)(A'+C)) \) convert to SOP

6. [BB] Algebraically convert the function \( H = W + Y'Z \) to a canonical sum showing intermediate steps. (Question: From the eqn. above, is \( H \) a function of \( X \)?) (8 pts.)

7. [BB] Complete the waveform for the circuit below. (10 pts.)

8. [BB] SOP vs. Canonical Form (18 pts.)
   a. Converting the circuit below to an equation and then find the minimal (smallest) SOP form. Hint: Use DeMorgan’s Theorem to simplify this a bit.
   b. Now expand your minimal SOP form to a canonical sum (sum or minterms).
HW 2b Paper Submission

9. [PAPER Submission] Reference the article [http://www.spectrum.ieee.org/semiconductors/design/the-hunt-for-the-kill-switch](http://www.spectrum.ieee.org/semiconductors/design/the-hunt-for-the-kill-switch) which discusses the possibility of unintended, unequivalent changes to a design. Below is a schematic for a “golden” design that we want to build. After running the design through certain CAD tools and giving it to the manufacturer, they return a “revised” design that they claim is equivalent. Determine if the “golden” and “revised” are equivalent. If they are not equivalent, fix the “revised” design by adding or removing at most 1-2 gates. You must derive an equation for the revised design and manipulate it to determine its equivalence. You are not allowed to generate truth tables. Hint: It will help to derive the AND-OR-NOT form of an XOR & XNOR function. (8 pts.)

![GOLDEN Design](image1)

![REVISED Design](image2)