Fall 2014 Syllabus **EE 101** Redekopp

Introduction to Digital Logic

Abstract:
This course introduces digital logic design basics which are fundamental to all computers and other digital hardware. Number systems, Boolean algebra, and analysis and design of combinational and sequential circuits are covered. Practical design techniques along with theory and principles will be taught. While focus will be put on paper-pencil design techniques, basic computer aided design tools and FPGA's will be introduced in several lab modules.

Instructor Info:

Instructor:	Mark Redekopp	Office Hours:	M,W: 10 – 11:30 W: 2-3
Office:	EEB 222		Th: 3:30-4
E-mail:	redekopp@usc.edu	Office Phone:	(213) 740-6006

TA's and Grader Info:

TA:	Fenxiao Chen Jason Tran Pedro Henrique De Silva	Grader:	Samatha Gavva Preethi Bhargavi Sama
Office:	See Blackboard	Office:	None
Office Hours:	See Blackboard	Grading Q's:	E-mail to setup appt.
E-mail:	fenxiaoc@usc.edu jasonatran@gmail.com pdasilva@usc.edu	E-mail:	gavva@usc.edu psama@usc.edu

Course Materials and Info:

Online Content (Blackboard):	http://blackboard.usc.edu (use your e-mail username and password)
Online Q&A	https://piazza.com/class#fall2014/ee101
Online Lecture Videos	http://marksee101.appspot.com
Class Notes (Required):	Available at the Bookstore
References (**NOT** Required):	"Digital Design", by Frank Vahid (ISBN: 0470044373) "Digital Design Principles and Practices" 4th Edition, by J.F. Wakerly (ISBN: 0131733494)

Grading Policy:

Participation and Homework	7% (lowest HW thrown out)
Labs	20%
Midterm 1	15%
Midterm 2	25%
Final Exam	30%
Office visit	3%

Homeworks: *Homeworks are your key to learning*. Only by doing problems on your own will you develop the logic skills and understanding to perform well on exams. You are expected to *present your own work with your own creative solutions.* **Experience has shown that those students who put in the effort on these homeworks, struggled with problems, asking questions when they did not understand a problem, did the best in this course.**

Homework should be submitted (usually via Blackboard) by the date posted on Blackboard. Any hard copy submissions should be neatly printed and be **stapled** together. If not due on Blackboard, a hard copy submission is due at the **beginning** of class. All circuit drawings should be neatly in Xilinx. **Late homework will be accepted with a 15% deduction**

per day and should be slipped under my office door. **Homework will not be accepted after solutions are posted** (2 days after the due date.) If you cannot make it to a lecture, turn it in early or have a friend turn it in. You will be expected to have read the listed sections of the class notes and textbook before each lecture.

Discussion/Lab: Discussion sections will be a mix of review/example problems and small lab exercises. Lab exercises will consist of small logic designs using a digital training board, FPGA boards, and logic simulators. These lab exercises are meant to give students an opportunity to work with actual hardware and provide concrete examples to the pencil and paper designs discussed in lecture. FPGA boards will be checked out to every pair of students. You are responsible for keeping these safe and undamaged. Lost or damaged boards will need to be paid for by the student(s) to whom it was checked out.

Exams: All exams will be closed book. The two midterms will be taken in the Quiz section (which is the only time we will use that slot) tentatively scheduled for the given dates. There will be no calculators allowed, just bring a few pencils and an eraser. You must show how you arrived at your answers to receive full credit. Any cheating may result in an "F" in the course and will be referred to Student Affairs for other penalties. Make up exams will only be given for valid medical or family emergency excuses (proof required).

Attendance and Participation: Attendance is mandatory to all lectures and discussions (even the morning ones). Rather than taking attendance, after selected lectures your attendance and participation will be measured using the following tools:

- Occasional Blackboard assessments. These online assessments will pose questions from the previous lecture or ask you questions on a reading assignment for the upcoming lecture. They will be posted at least 24 hours before class and may be completed anytime before class.

Office visits: You will receive 3% of your course grade for making an office visit *before the drop date, Nov. 14th*. This is designed to help me better know you and your interests.

Expectations: Attend lectures, do your homework, BE CURIOUS!

Academic Integrity: Academic integrity is critical the assessment and evaluation we perform which leads to your grade. In general, all work should be your own and any sources used should be cited. Gray-areas occur when working in groups. Telling someonw how to do the problem or showing your solution is a VIOLATION. Reviewing examples from class or other sources to help a fellow classmate understand a principle is fine and encouraged. All students are expected to understand and abide by these principles. SCampus, the Student Guidebook, contains the University Student Conduct Code in Section 10, while the recommended sanctions are located in Appendix A. Students will be referred to the Office of Student Judicial Affairs and Community Standards for further review, should there be any suspicion of academic dishonesty.

Academic Accommodations: Any student requiring academic accommodations based on a disability is required to register with Disability Services and Programs (DSP) each semester. A letter of verification for approved accommodations can be obtained from DSP. Please be sure the letter is delivered to me as early in the semester as possible. DSP is located in STU 301 and is open 8:30 a.m. - 5:00 p.m., Monday through Friday. The phone number for DSP is (213) 740-0776.

This class may seem mundane for the first few weeks but it will pick up pace quickly. Please do not fall behind early!

EE 101 Schedule and Topics (W = Wakerly, LN = Lecture Notes)

Wk	Tuesday	Thursday	Readings	Lab/Disc
1	Analog vs. Digital Positional # Systems	Number Conversion Binary, Octal, Hex Binary Codes: ASCII, BCD Binary Arithmetic	**W**: Ch. 1, 2.1-2.4, 2.10, 2.12 **LN**: 1-28	Review
2	Signed Magnitude 2's complement System Sign Extension	**The Basics**: Logic Functions & Representation Minterms / Maxterms Canonical Sums/Products	**W**: 2.5,4.1 **LN**: 29-51	L1: Alarm
3	**The Tools**: Boolean Algebra (T1-T5) Boolean Algebra (T6-T11) DeMorgan's Theorem	**Circuit Analysis** Waveforms (maybe timing) Conversion to Canonical Form	**W**: 4.1,4.2 **LN**: 51-82	Review
4	Design Goals Circuit Design, Manipulations, 2-Level Implementations **Circuit Synthesis** Canonical Implementation	Simplified 2-Level Impl. Karnaugh Maps Don't Cares Decoders & Muxes & ROM's	**W**: 4.3, 9.1 **LN**: 83-125	L3: K-Maps
5	More Circuit Design	Decoders (Enables, Active Levels, Composition)	**W**: 6.1, 6.4 **LN**: 126-140	L4: Xilinx
6	Encoders Multiplexers (Composition, Width)	Multiplexers Demultiplexers Adders	**W**: 6.5, 6.7, 6.10 **LN**: 140-156	Review
Midterm 1 - 10/3				
7	Adders Multipliers	Addition/Subtraction Overflow	**W**: 6.10-6.11, 2.5-2.6 **LN**: 157-182	L5: CLAs
8	Comparators XOR's & Parity	Sequential Logic Bistables	**W**: 6.9, 6.8,6.6,7.1 **LN**: 183-195	L5: CLAs (cont)
9	Latches Flip-Flops	Master/Slave FF's Review	**W**: 7.1, 7.2 **LN**: 195-222	L6: FPGAs
10	State Machine Overview State Machine Analysis	State Machine Design State Machine Analysis	**W**: 7.2-7.3 **LN**: 223-233	Review
Midterm 2 – 10/31				
11	State Machine Design Registers Registers W/ Enables	Counters Digital System Design	**W**: 7.3-7.5 **LN**: 234-255	L7: Crosswalk
12	Datapath & ALU design	System Design (Vending Machine)	**W**: 8.2, 8.4, 8.5 **LN**: 255-280	L8: Vending Machine
13	CPU Design	CPU Design	-	L8: cont.
14	Filter Design	Thanksgiving	-	Holiday
15	JPEG Encoding	Final Review	-	L8: cont.
Final Exam (Cumulative): Mon., Dec. 15th from 4:30-6:30 p.m. Location TBA				

* Schedule (especially lab schedule) is subject to change. See announcements on Piazza *