Non-Volatility For Ultra-Low Power Asynchronous Circuits in Hybrid CMOS/Magnetic Technology

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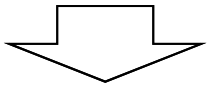
Outline

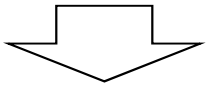
- Motivation & Background
- Non-Volatile C-element
- Asynchronous Non-Volatile circuits
- Summary & Conclusion

Motivation & Background

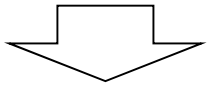
Internet-of-Thing is an extensively spreading technology that creates a lot of opportunities for the variety of normally-off devices



Severe constraints: power consumption, autonomy, changing energetic environment



Robust circuit with instant off/on capabilities and low power

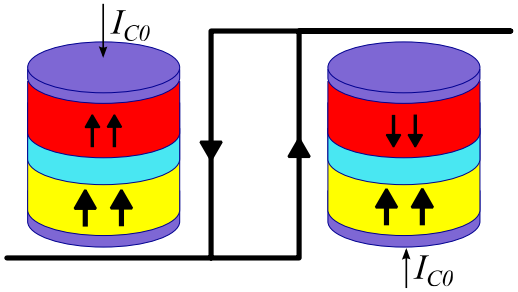


Can be efficiently implemented using the following technologies/approaches

Motivation & Background

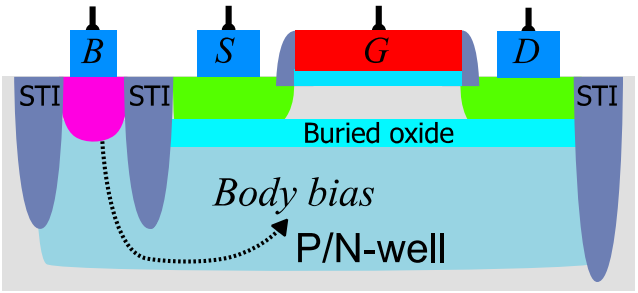
Internet-of-Thing is an extensively spreading technology that creates a lot of opportunities for the variety of normally-off devices

MRAM based Non-Volatile memory



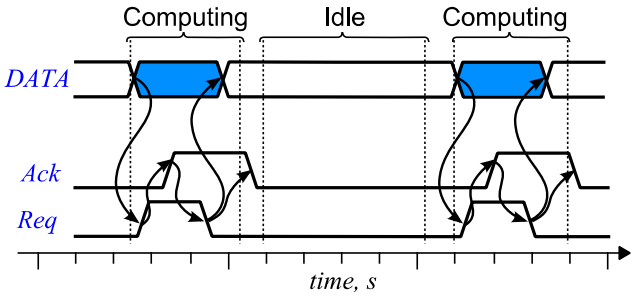
- Instant on/off
- Robustness toward unstable energetic environment
- Zero consumption in offline mode

Fully Depleted Silicon on Insulator CMOS technology



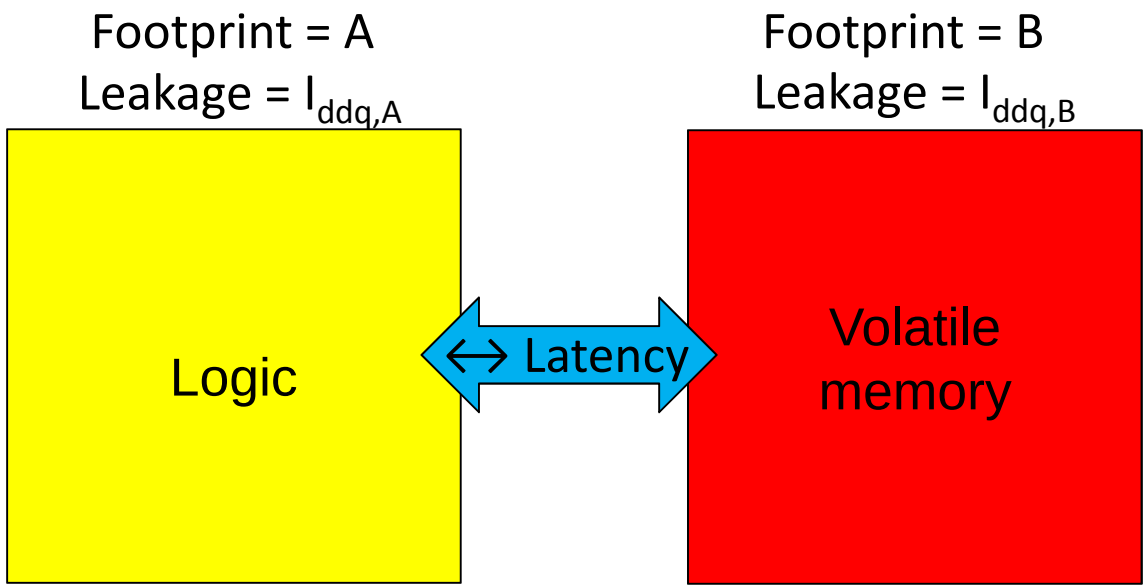
- Wide supply range
- Robustness toward PVT
- Low power consumption

Asynchronous communication



- Lower supply voltage
- Natural automatic on/off
- Robustness toward PVT

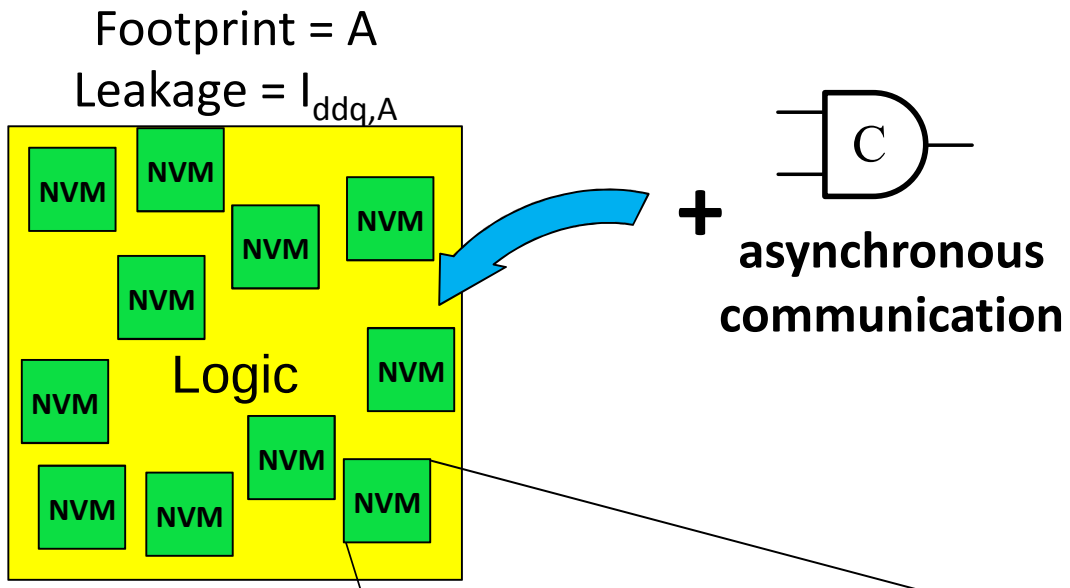
Background: Logic-in-Memory & Integration



Von Neumann architecture:

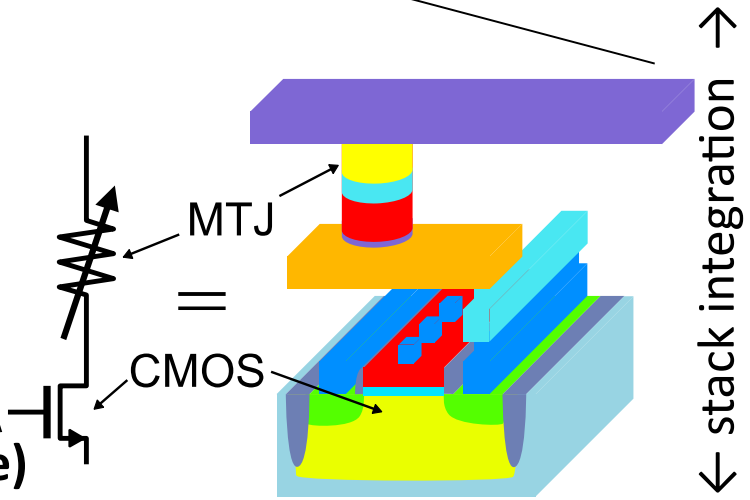
- **Large footprint (A + B)**
- **High dynamic & static losses**
- **Latency**
- **Complex layout**

Background: Logic-in-Memory & Integration



Logic-in-Memory architecture:

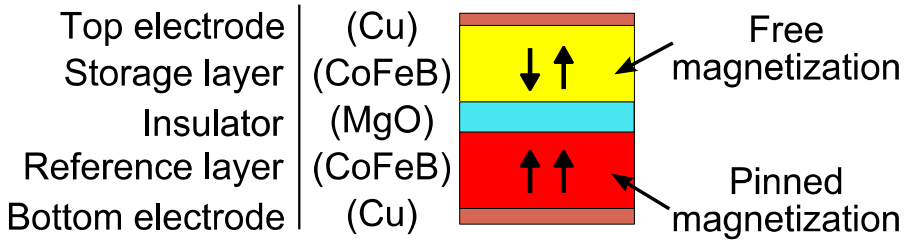
- **Small footprint (A)**
- **Reduced latency**
- **Quazi-zero static power**
- **Reduced dynamic power (incl. backup+restore)**



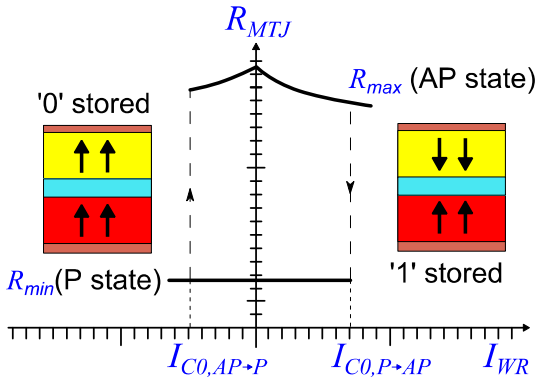
Background: Magnetic memory (STT-MRAM)

Why magnetic memory?

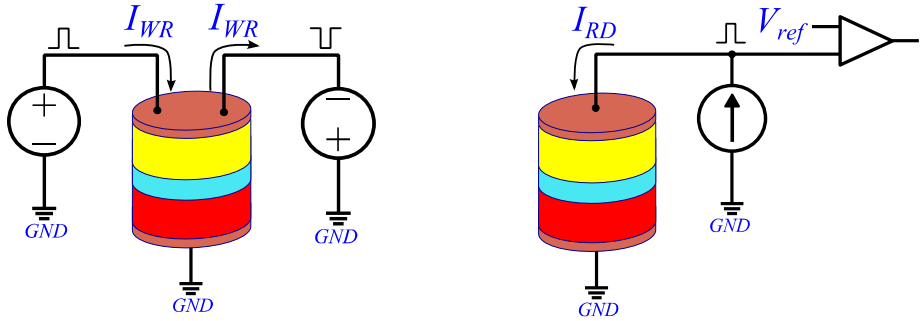
- **Non-volatile: no leakage**
- **Fast R/W: ns range**
- **High endurance: > 10 years**
- **Low R/W energy : tens of fJ range**
- **Low R/W voltage: < 500 mV**
- **Easy to embed: e.g. in BEOL**
- **High density: < 40 nm**



Basic component: Magnetic Tunnel Junction (MTJ)



Resistance vs storage layer magnetization

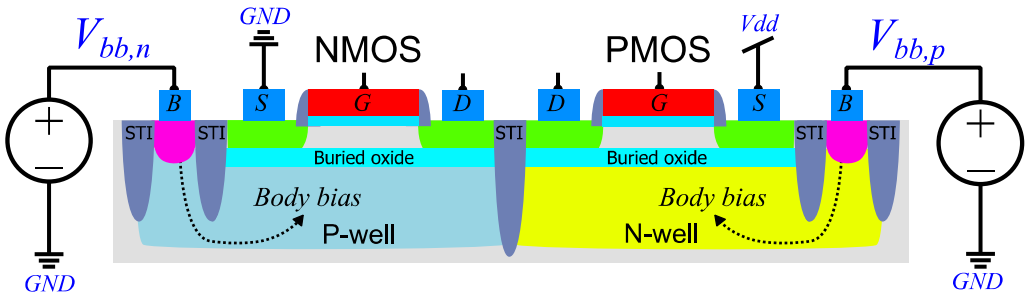


Write ‘1’ Write ‘0’ Read

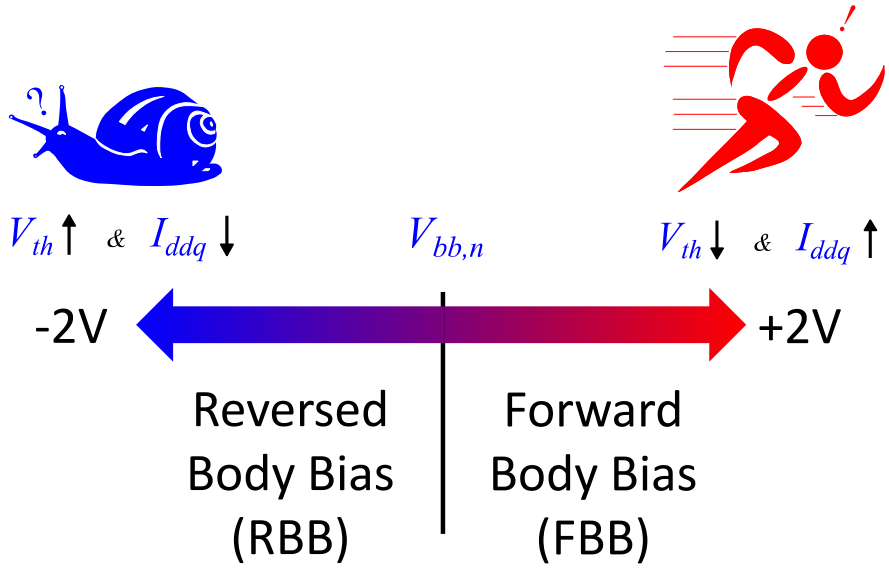
Background: FD-SOI technology

Why FD-SOI technology?

- **High performance/lower power**
- **Low variability**
- **Advanced power/speed control features**



Cross section view of FD-SOI transistors



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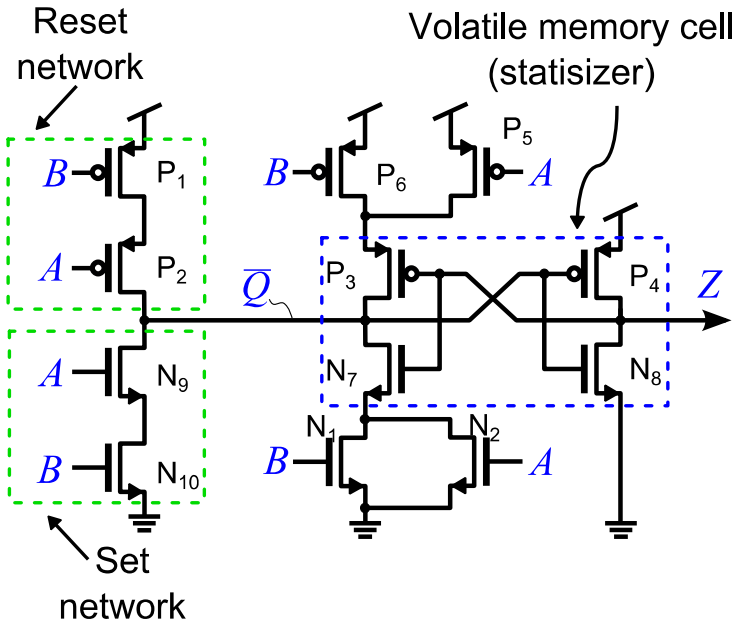
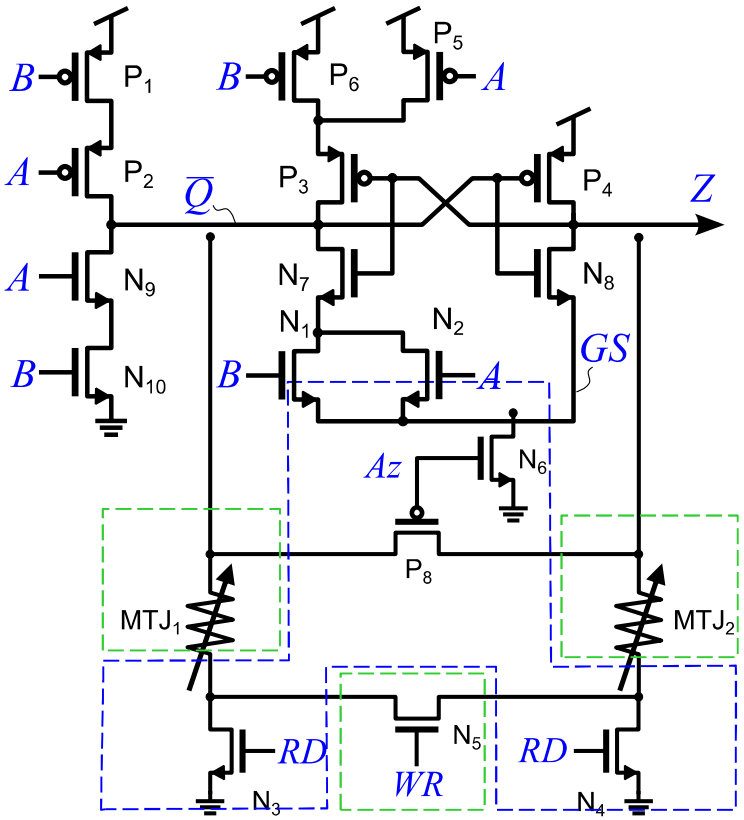
Non-volatile C-element: schematic

Conventional volatile C-element
(Muller gate)



state is lost @ power gating !

Proposed non-volatile cell

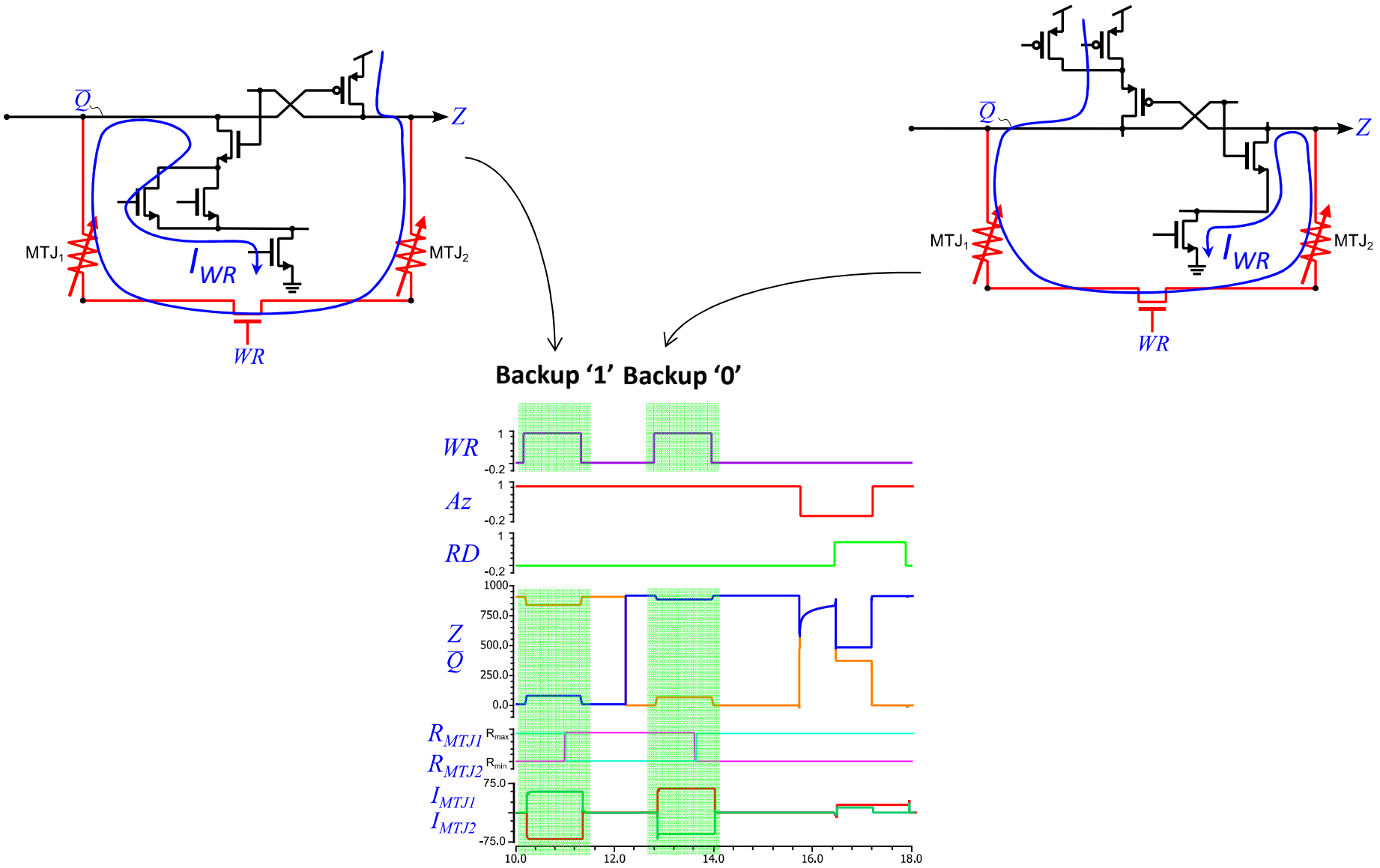


+ 2MTJ for differential NVM

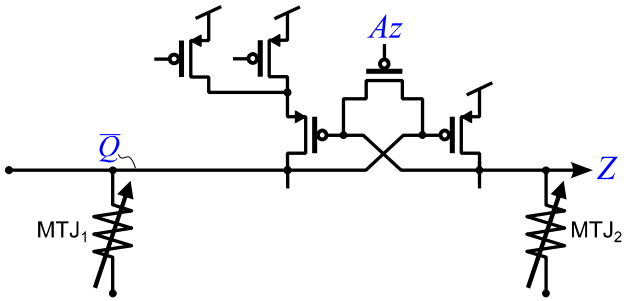
+ 4T for read procedure

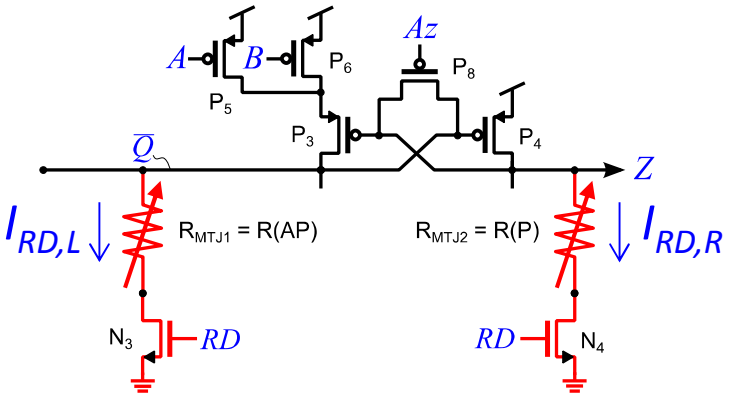
+ 1T for write procedure

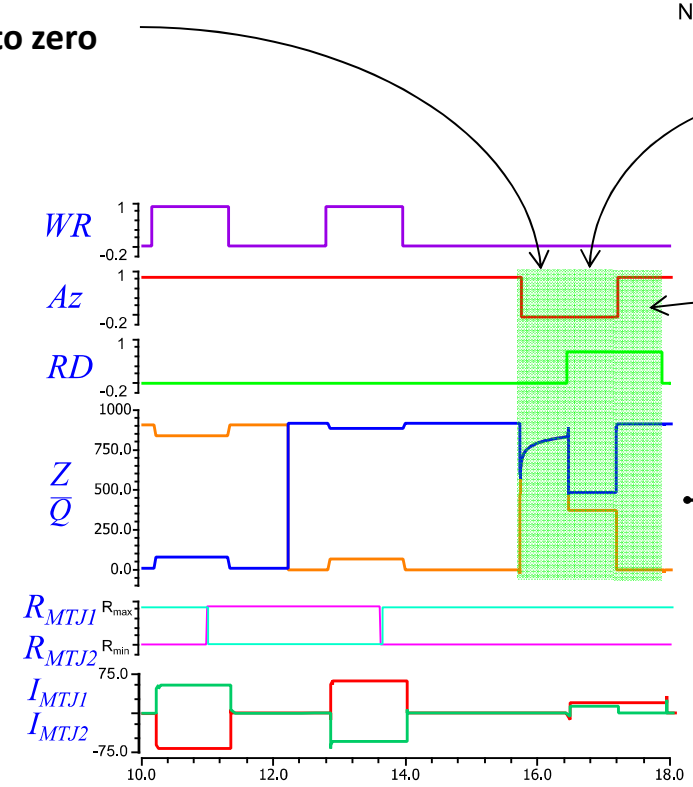
Non-volatile C-element: write principle

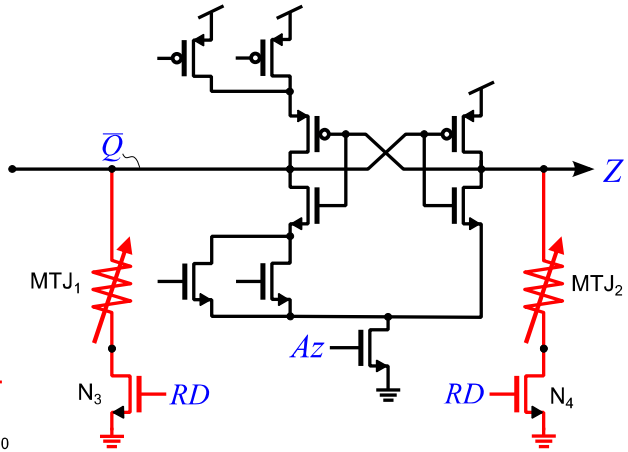


Non-volatile C-element: read principle









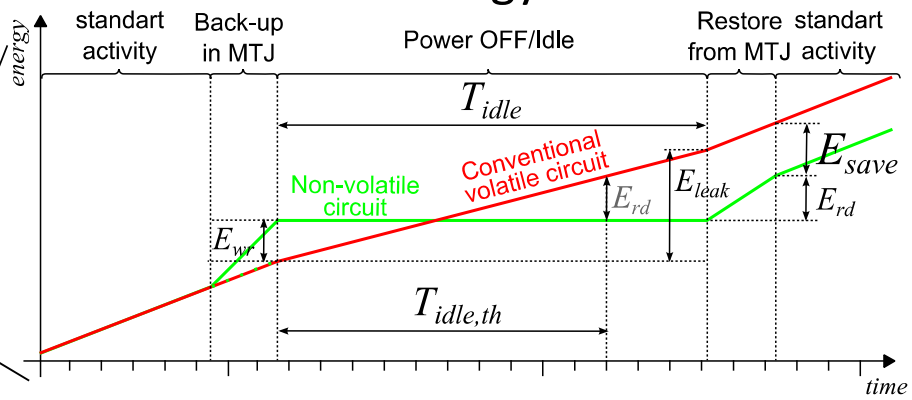
Non-volatile C-element: energy efficiency

Results of the simulations of the standard and NV cells in 28 nm FDSOI technology (LVT)

Parameter	no BB		with BB	
	STD cell	NV cell	STD cell	NV cell
Delay time, ps	19	46	13	32(1)
Leakage current, nA	12.1	28.5	7.1(3)	16.9(3)
Idle power, nW	11.1	26.2	6.5(3)	15.5(3)
$Vdd_{min,cmos}$, mV	498	498	160(1)	160(1)
$Vdd_{min,mag}$, mV	-	845	-	643(1)
WR energy E_{WR}, fJ	-	50	-	42(2)
RD energy E_{RD}, fJ	-	15.7	-	13.7(3)
Time $T_{idle,th}$, us	-	6	-	8.8
Area, um^2	1.2×1.2	1.2×2.6	1.2×1.2	1.2×2.6

(2)+2 V FBB
(1)+0.7 V FBB (optimal)
(3)-0.3 V RBB

Efficiency criteria: threshold time when leakage energy ≥ NVM Write+Read energy



$$T_{idle,\,th} = \frac{E_{WR} + E_{RD}}{E_{leak}/T_{idle}}$$

- **Ultra-low voltage operation in standard mode: down to 160 mV**
- **Low voltage operation in NV mode: 30% lower than nominal supply**
- **Body Bias reduces the cost of NV feature: roughly by 15%**
- **NV upgrade is reasonable if idle periods are longer than 10 us**
- **Gate delay penalty is x2 and not an issue for the autonomous application**

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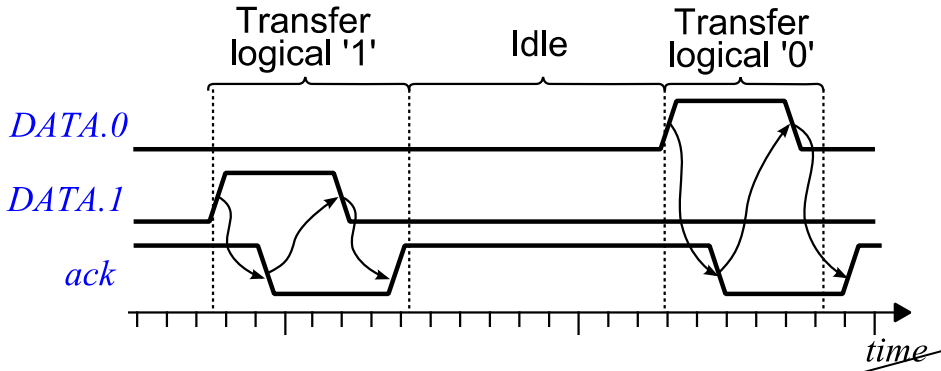
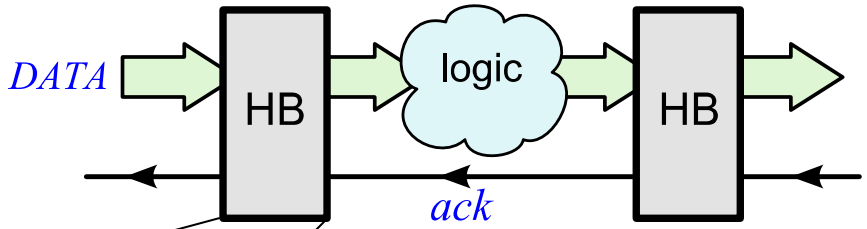
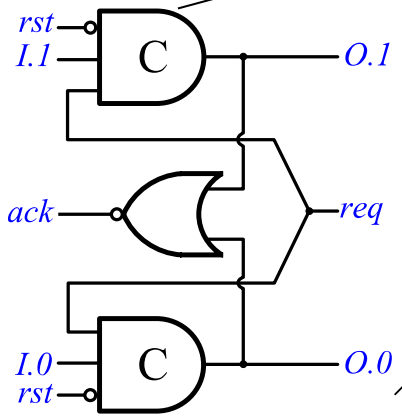
Asynchronous NV circuits: Half-Buffer

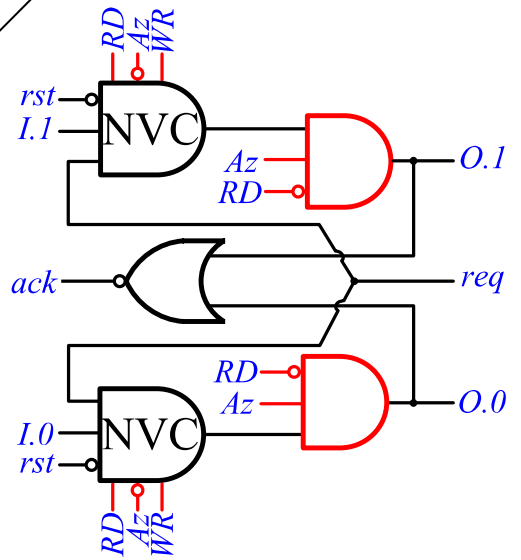
Case study: asynchronous 4 phase handshake dual rail protocol for Quasi Delay Insensitive (QDI) circuits





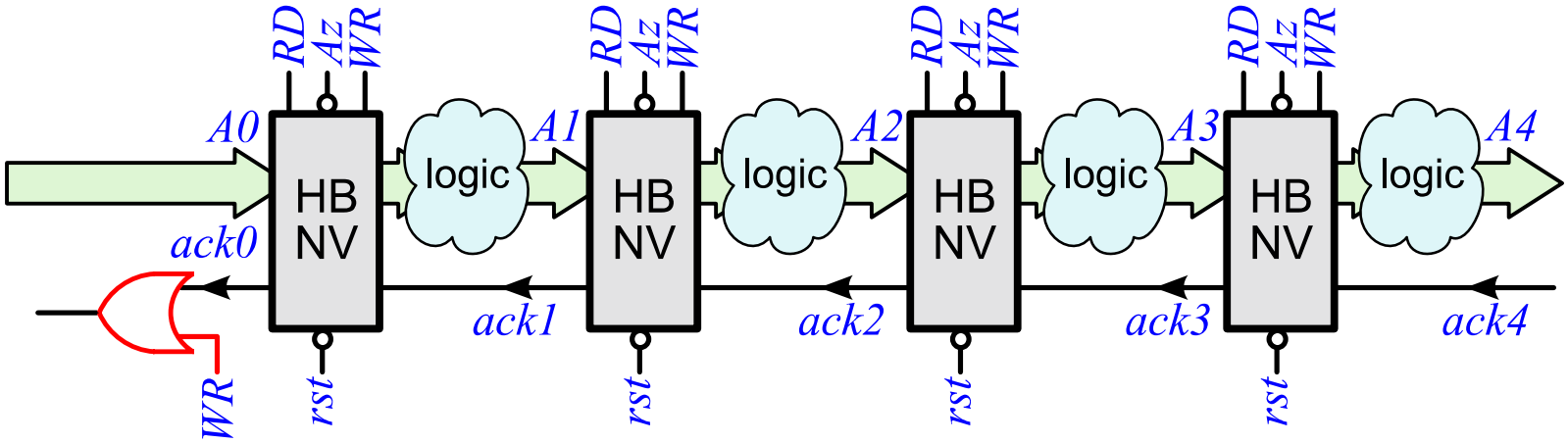


Conventional Half-Buffer in asynchronous pipeline



Proposed Non-Volatile Half-Buffer

Asynchronous NV circuits: pipeline



Issues of NV implementation:

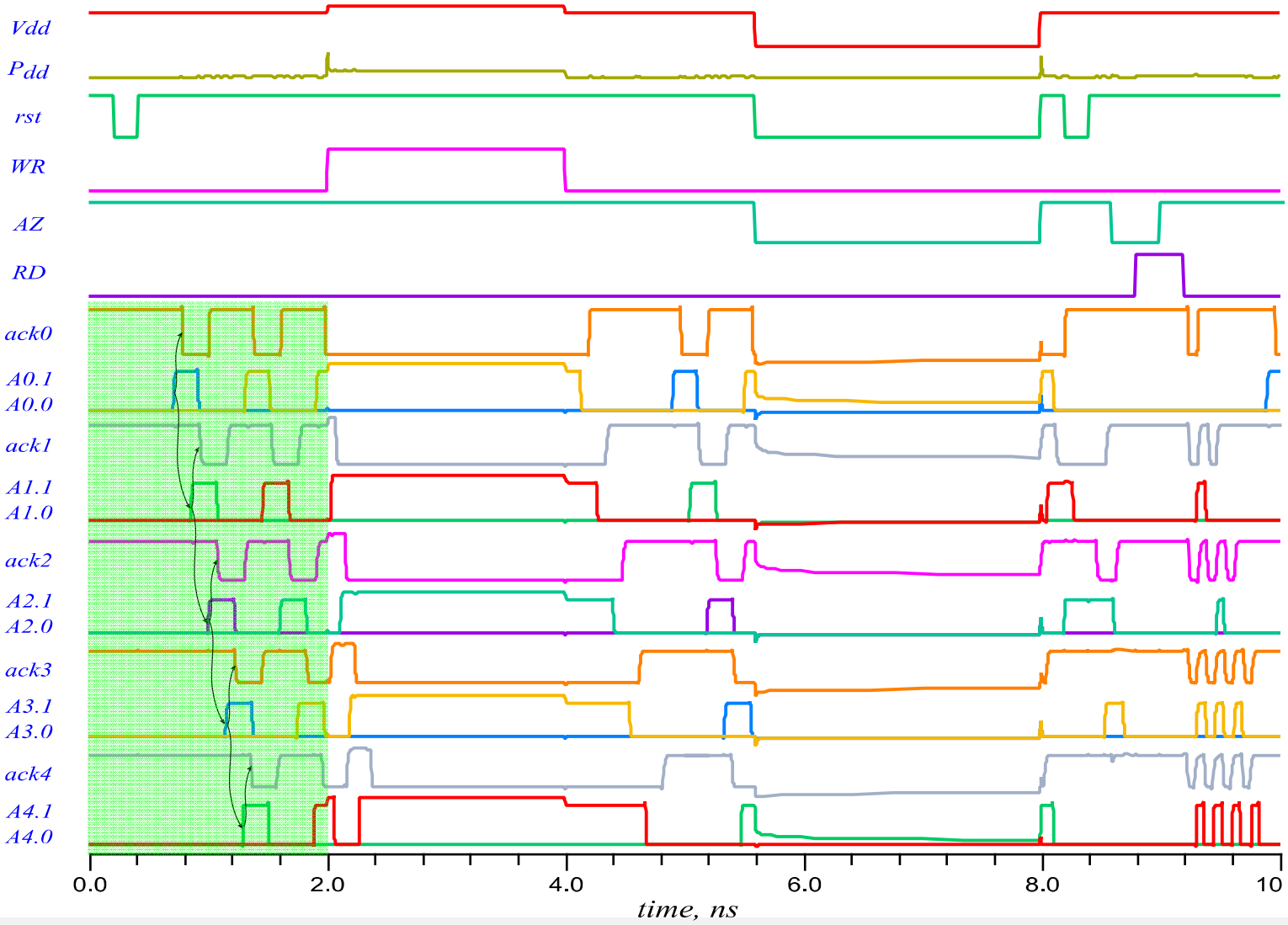
- **Synchronization of backup/restore with basic asynchronous operation of HB**
- **STT-MRAM writing time is significant comparing to data hold time (1-2 orders)**

Proposed algorithm:

- **Freeze the pipeline by gating the acknowledgment signal(s) (ack → '1')**
- **Keep the freeze state for a time, sufficient for the writing in NVM (e.g. T_{wr} > 10ns)**
- **Release the acknowledgment signal and continue normal operation**

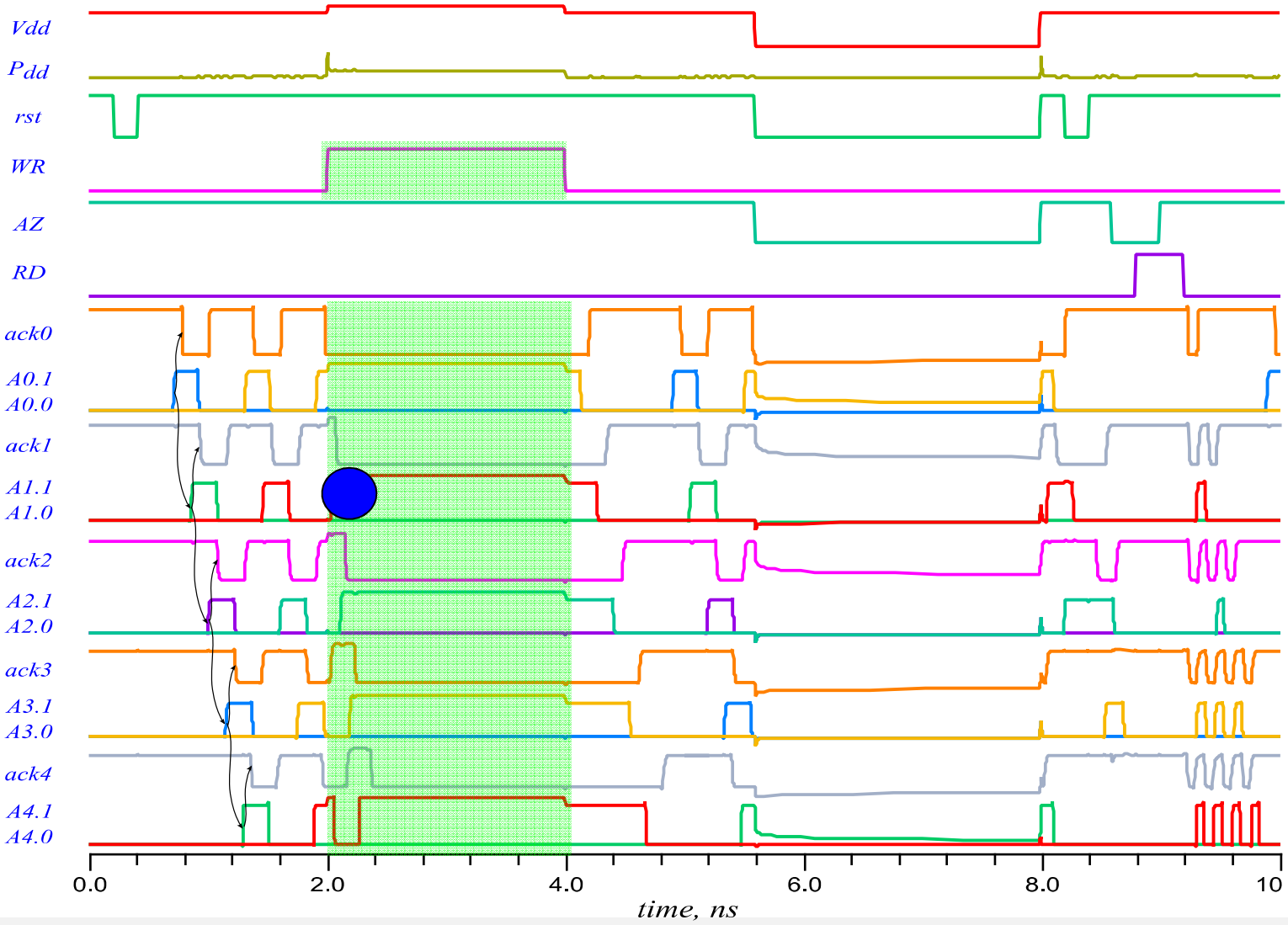
Asynchronous NV circuits: pipeline simulation

Std operation mode



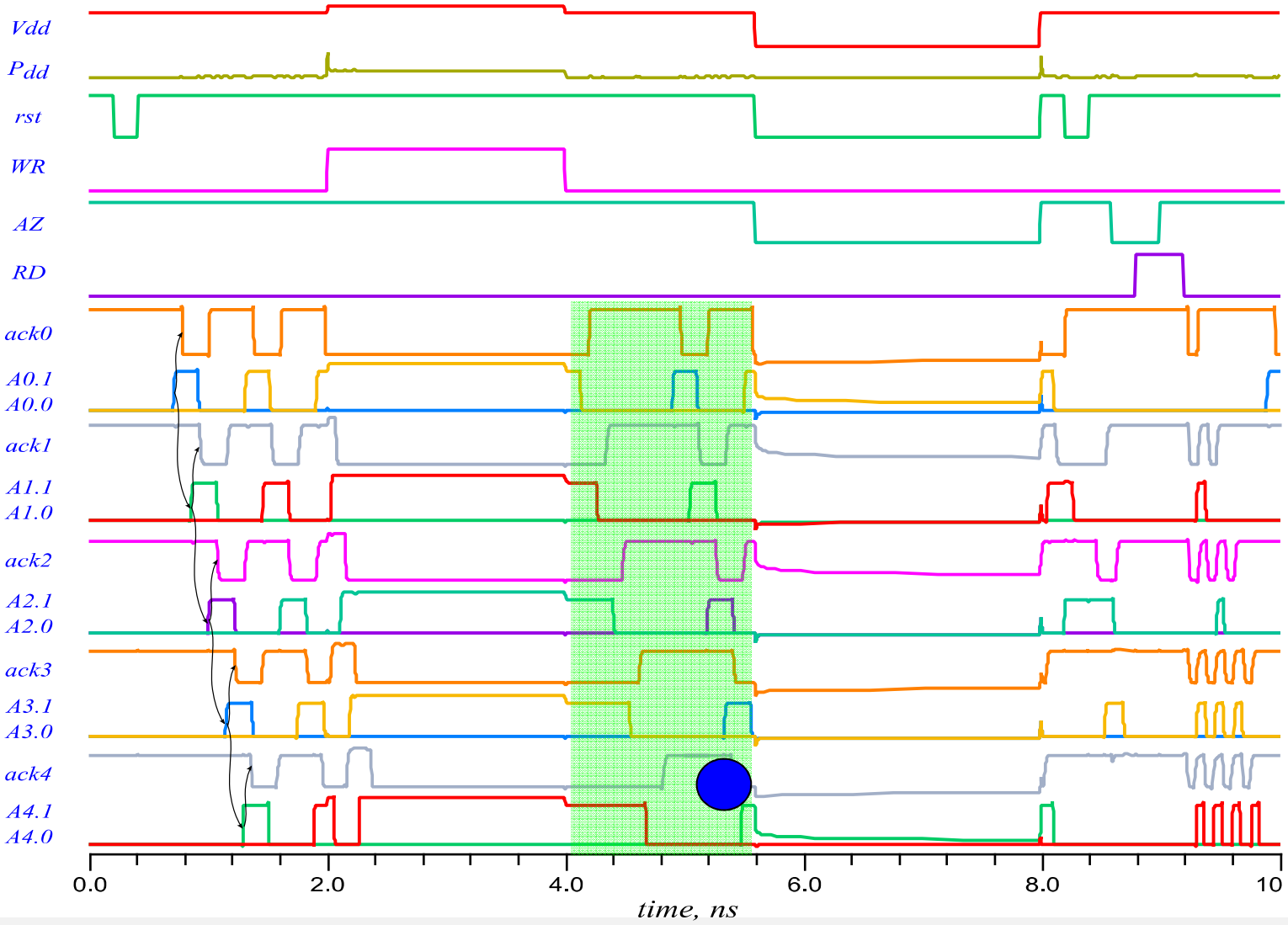
Asynchronous NV circuits: pipeline simulation

Backup in NVM (2ns)

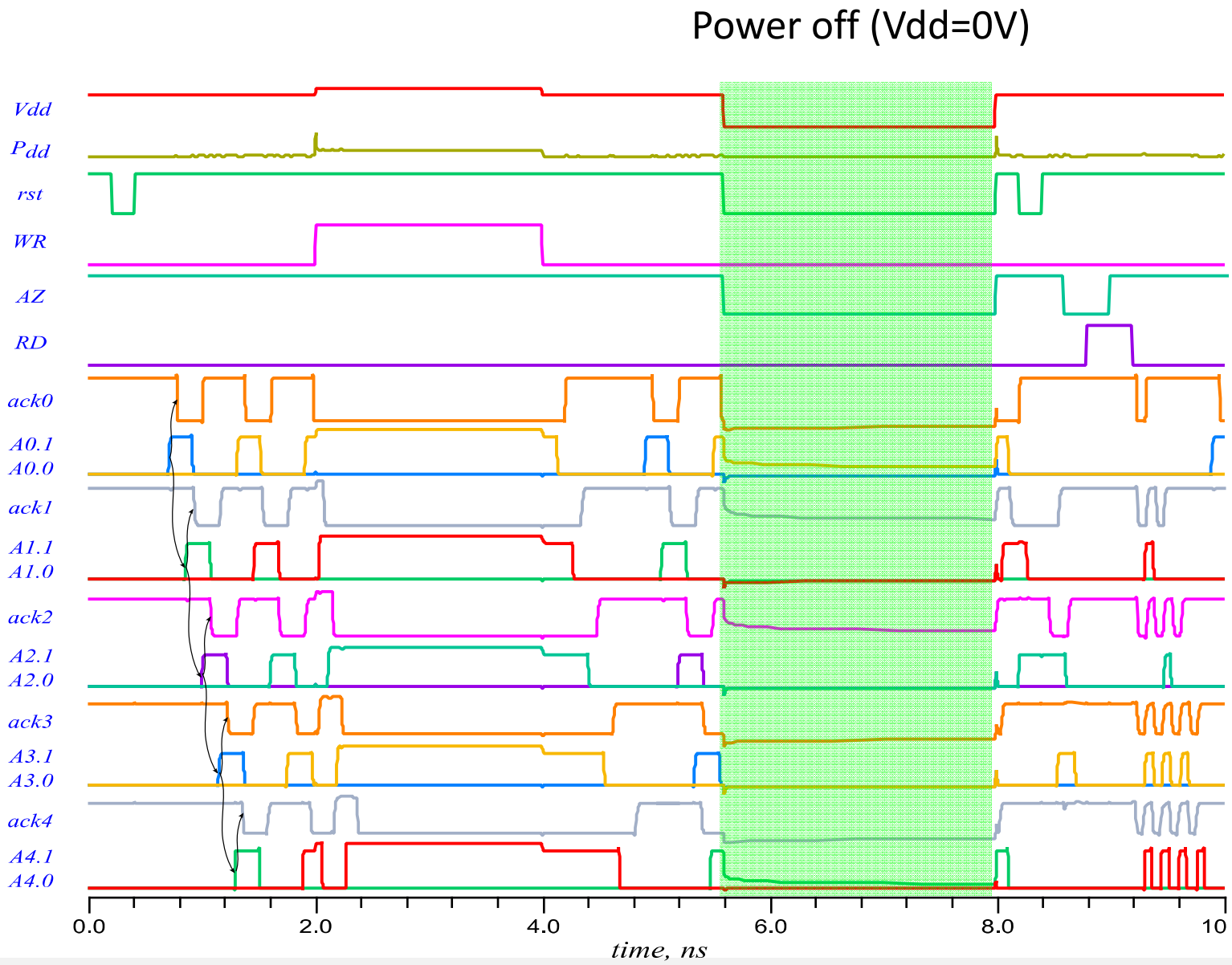


Asynchronous NV circuits: pipeline simulation

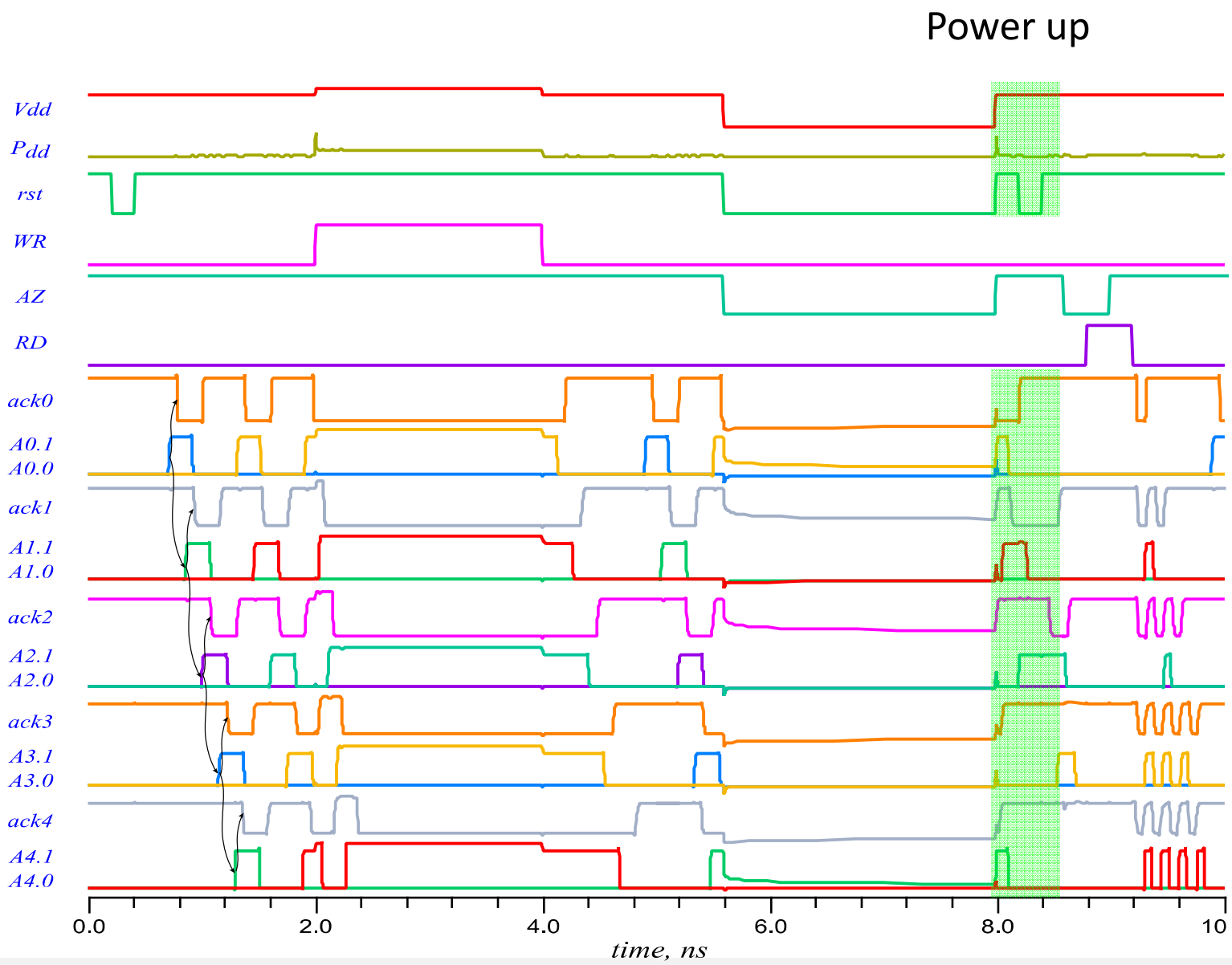
Continue std operation



Asynchronous NV circuits: pipeline simulation

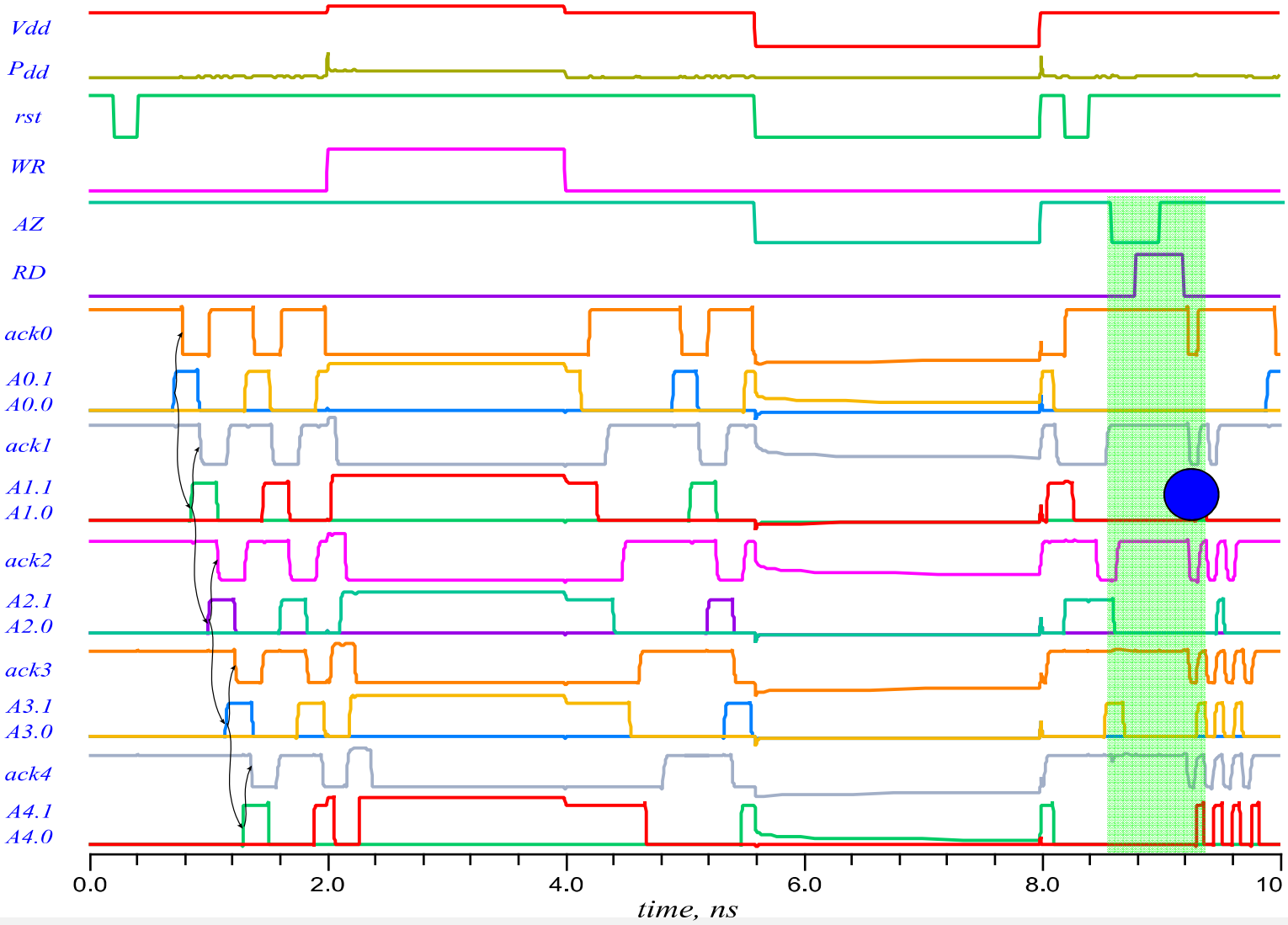


Asynchronous NV circuits: pipeline simulation



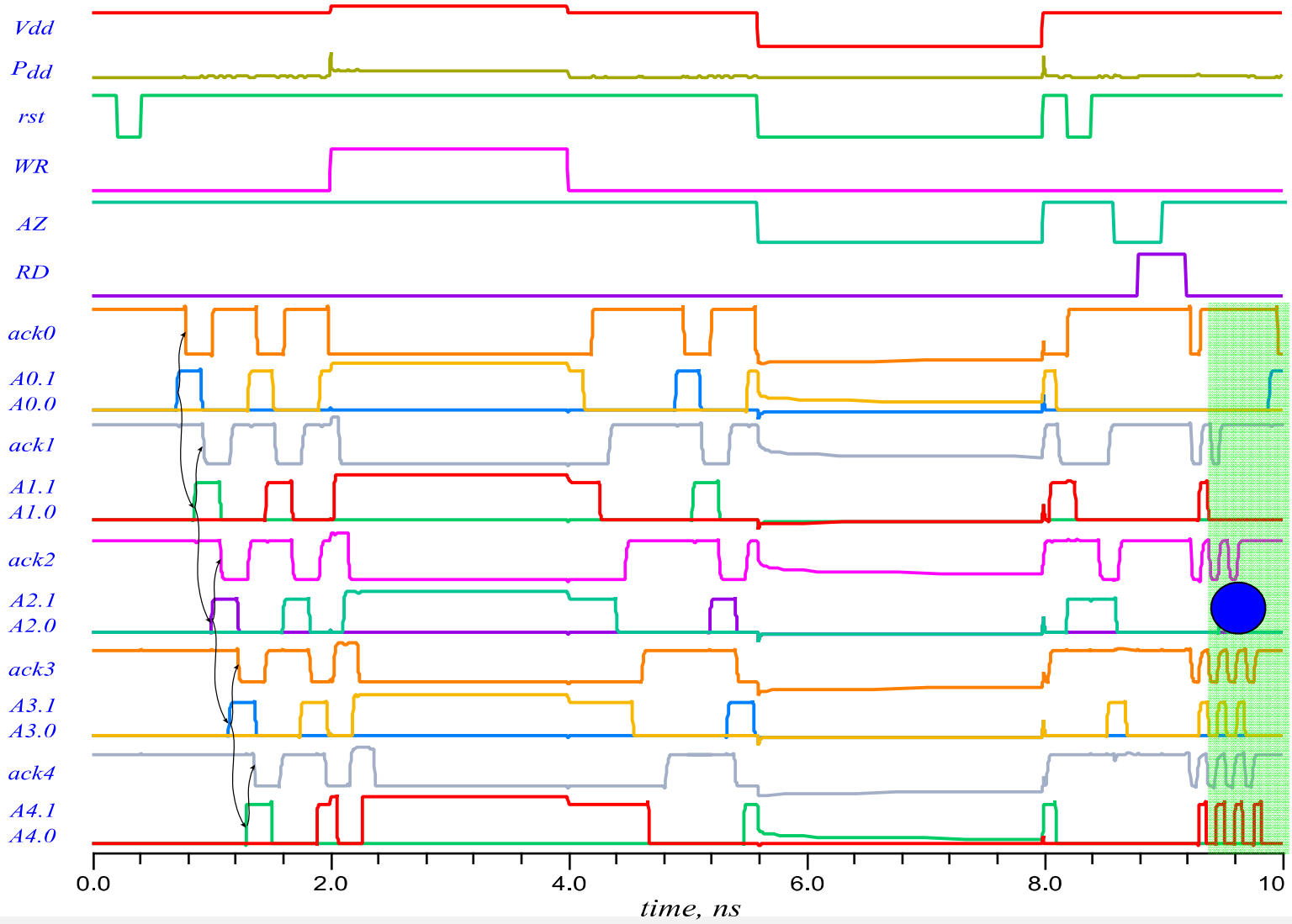
Asynchronous NV circuits: pipeline simulation

Recovery from NVM

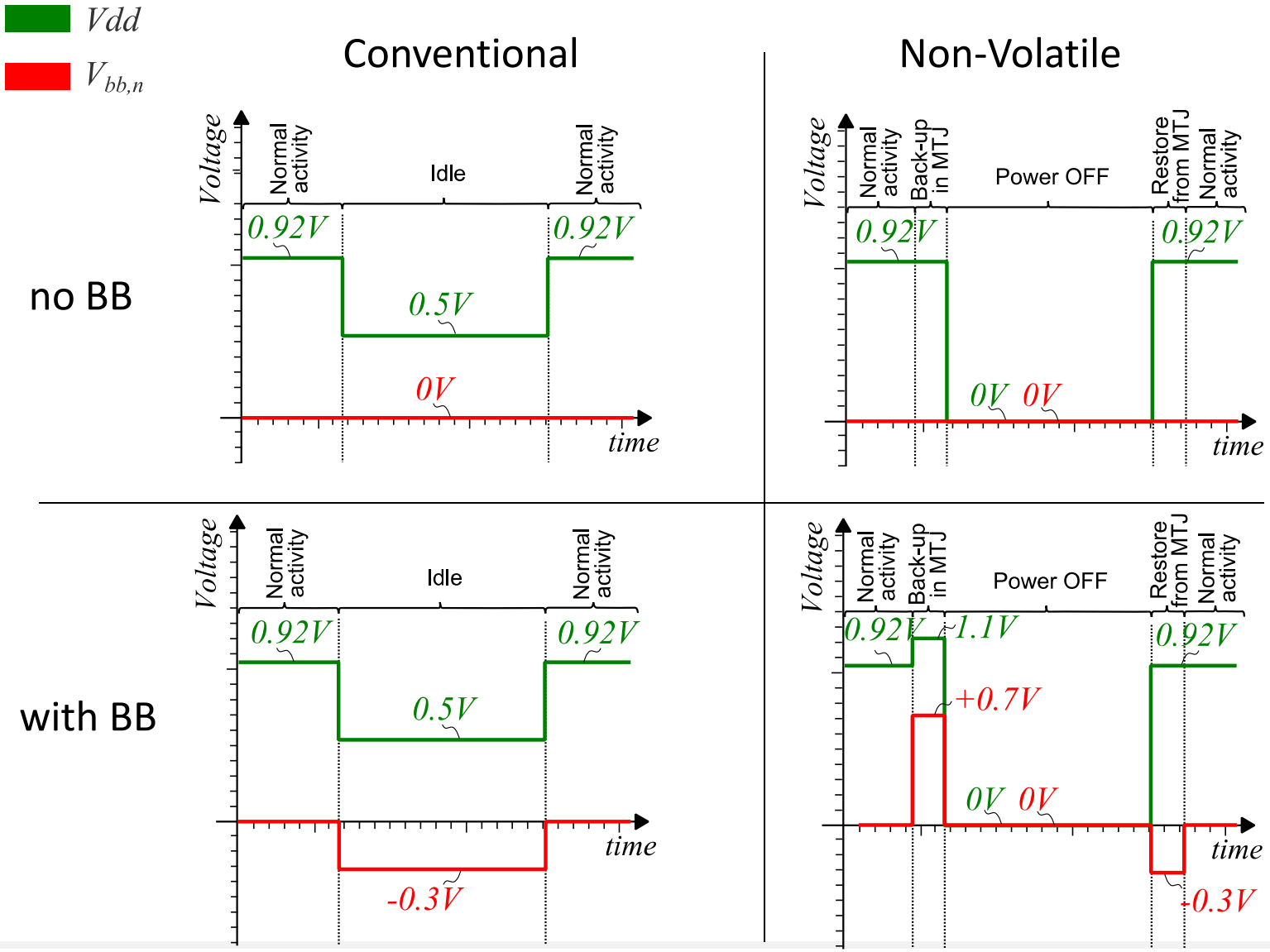


Asynchronous NV circuits: pipeline simulation

Resume std operation

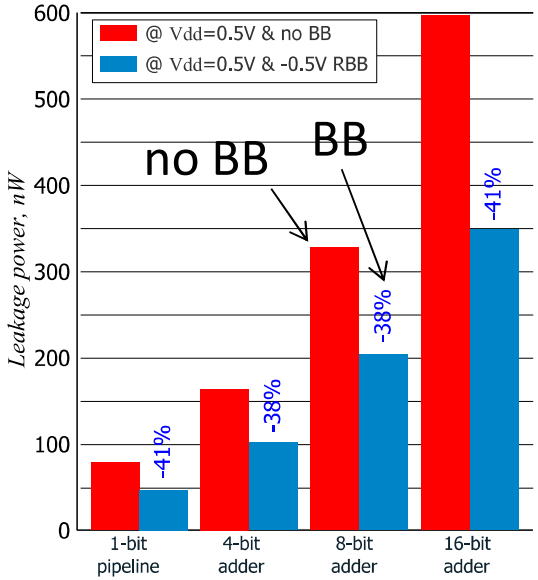


Asynchronous NV circuits: BB and supply control

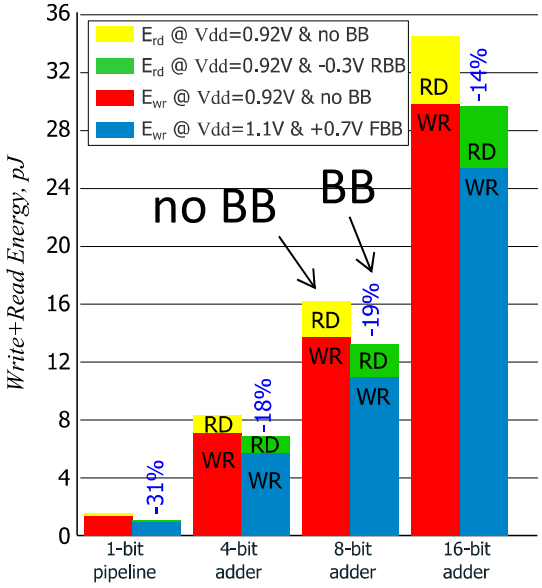


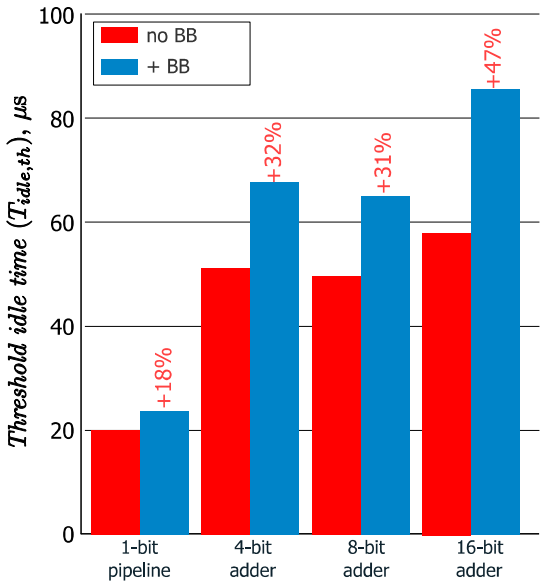
Asynchronous NV circuits: V vs NV tradeoff

Leakage power in conventional volatile circuit



Write + Read energy in non-volatile circuit





Volatile vs Non-Volatile tradeoff. NV functionality is reasonable if the idle time of the volatile circuit is greater than threshold time $T_{idle,th}$

Summary & Conclusion

- Magnetic memory brings non-volatility to asynchronous circuits for low-power and normally-off circuits of the Internet-of-Things applications:
  - The NV functionality is justified if the idle mode of the application is greater than few tens of microseconds
  - Delay penalty (>x2) of the NV cells due to the NV functionality is too high and requires optimizations
- Adaptive control over supply and body bias voltages can minimize the power consumption during dynamic operation, idle phases and backup:
  - Aggressive FBB permits to reduce the supply voltage in conventional mode down to 160 mV and in NV mode down to 643 mV
  - Optimal FBB can save from 14 to 30% of the energy during backup/restore
  - The RBB reduces the leakage current in all simulated circuits by 40%

Future work

- Circuit level optimizations: e.g. gate delay minimization
- Study self-adjusting solutions for minimum energy/delay
- Fine grain writing of the NVM using activity detection mechanism

Thank you for your attention

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* Questions are guaranteed in life; answers aren't.