Design and Analysis of Testable Mutual Exclusion Elements

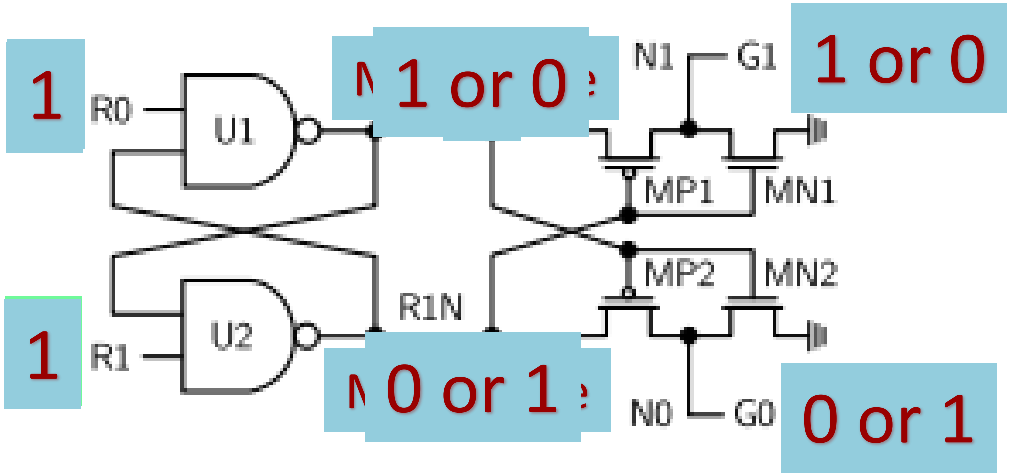
05/06/2015

Yang Zhang, Leandro S. Heck,
Matheus T. Moreira, David Zar, Mel Breuer,
Ney L. V. Calazans and Peter A. Beerel

Outline

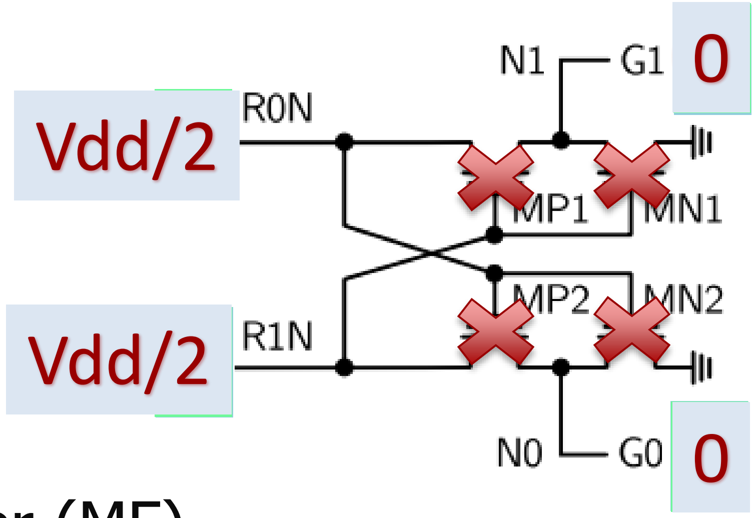
- Introduction
    - MUTEX and Its Operation
    - Motivation
- Proposed Testable MUTEX (Full-Custom)
    - Structure
    - Fault Coverage
    - Testable Metastability Filter
- Proposed Testable MUTEX (Standard-Cell)
    - Structure
    - Fault Coverage
    - Testable Metastability Filter
- Experimental Results and MetaACE Analysis of Settling Times

MUTEX and Its Operation



- Operation
  - Mutually exclusively raise grant (G0 or G1) in response to requests (R0 and R1)
- Metastability (MS)
  - Outputs of NAND gates may stay close to Vdd/2 for an unbounded amount of time

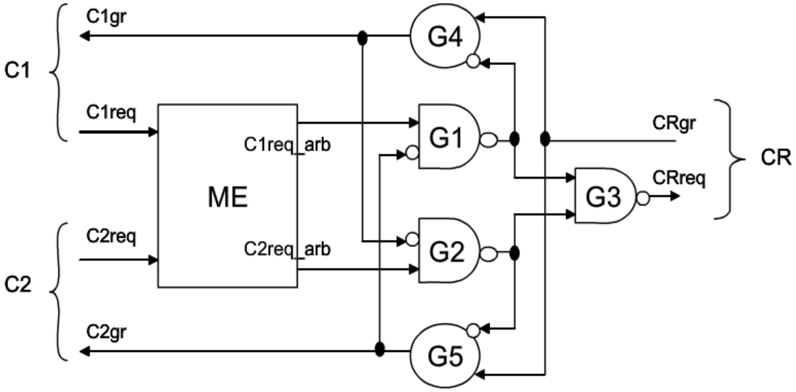
Metastability Filter



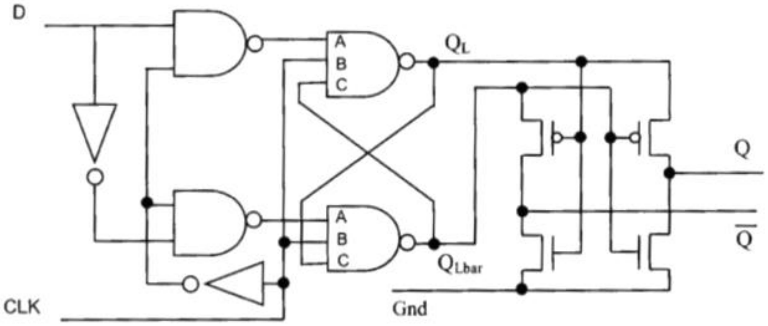
- Metastability Filter (MF)
  - Guarantee grant outputs (G0 and G1) remain stable 0 until MS is resolved
  - G0 to 1 only when R0N and R1N differ by more than V_t of PMOS transistors MP1/MP2

MUTEX Applications

- Pausible Clocking Circuits
  - Arbitrate b/w clock and pause signals
- Asynchronous Crossbar / NoC routers
  - Typically contains arbiters to decide the access to output ports
  - Arbiters contains MUTEXes
- Asynchronous Resilient Computing (Blade)
  - Relies on Q-Flop to sample error signal
  - Q-Flop contains a MUTEX
  - Async control waits for MS to resolve



Classic arbiter



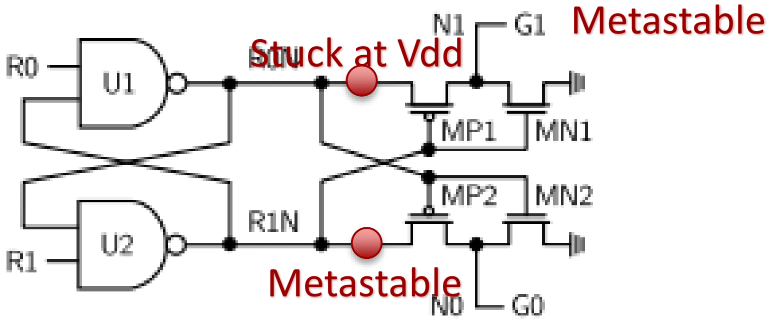
Classic Q-Flop

Motivation

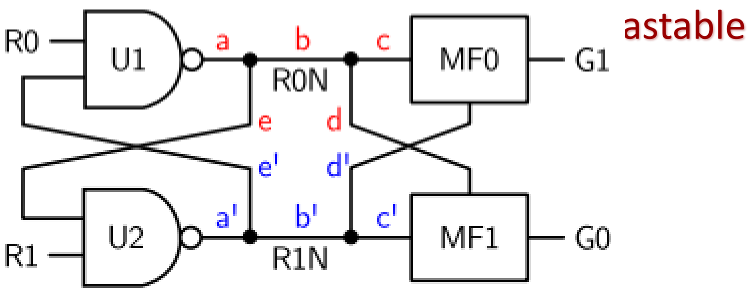
- Possible outcomes of metastability
  - Metastability can delay outputs significantly
  - Failure in Metastability Filter may allow metastability to propagate
- Functional testing is not sufficient
  - Hard to guarantee testing metastability due to fs-timing required
  - Miss testing key behavior of control circuits driven by MUTEXes

Failures may slip through

Drawback 1: Undetectable Stuck-At Faults



Full-custom MUTEX design



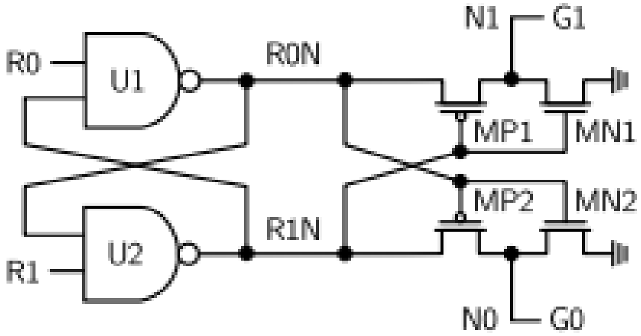
Gate-level model

Node	Test	Detectable	Test Vector {R0, R1}	Fault-free Output {G0, G1}	Faulty Output {G0, G1}
R0	SA0	Yes	{1, 0}	{1, 0}	{0, 0}
R0	SA1	Yes	{0, 0}	{0, 0}	{1, 0}
c	SA0	Yes	{0, 1}	{0, 1}	{0, 0}
c	SA1	No	–	–	–
c'	SA0	Yes	{1, 0}	{1, 0}	{0, 0}
c'	SA1	No	–	–	–
⋮					

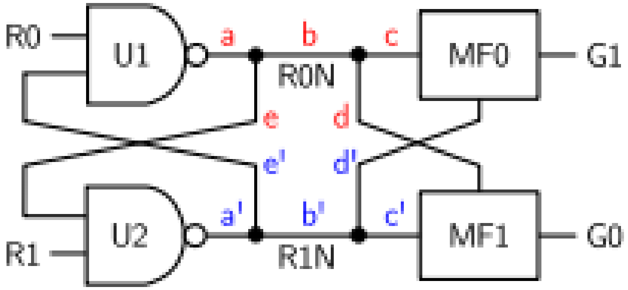
Stuck-At Fault Analysis for FC-MUTEX

- ❖ Two SAFs not detected
- ❖ Nodes c and c' stuck-at-1

Drawback 2: Non-testable MS Filter



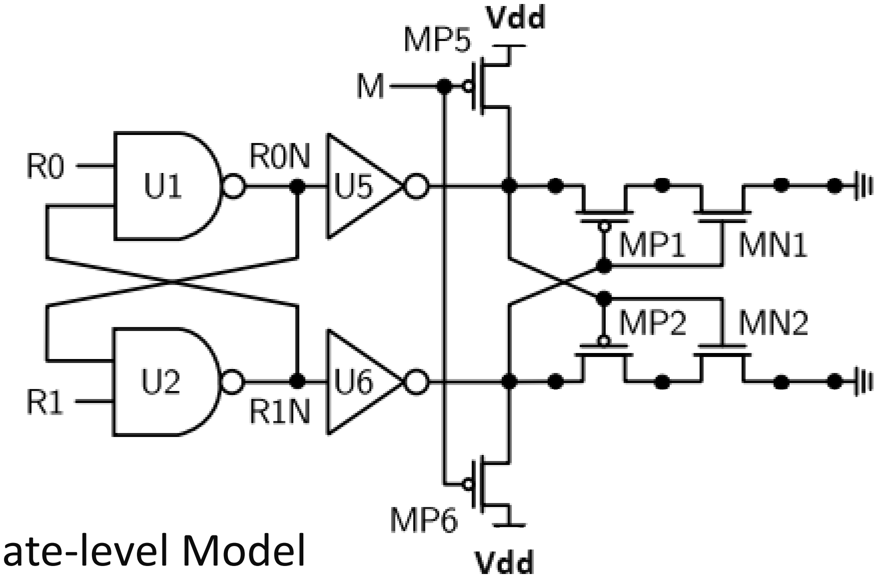
Full-custom MUTEX design



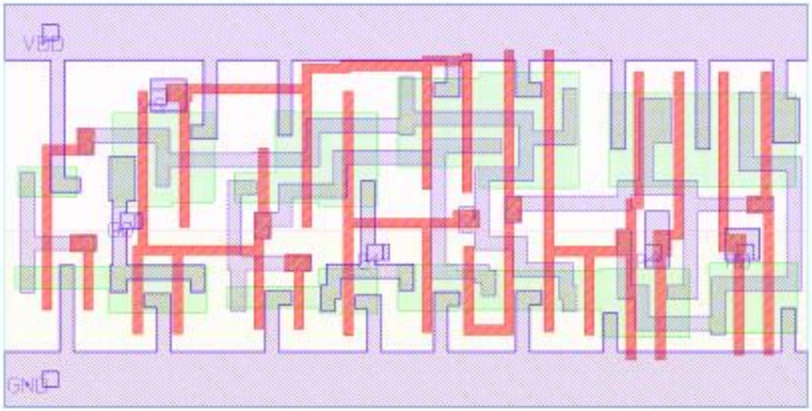
Gate-level Model

- No single test vector generates prolonged metastablility
- Test vector pair (R0, R1) = (0,0) → (1,1)
  - May generate MS but depends on exact input timing
  - May be short-lived

Proposed Testable MUTEX (Full-Custom)



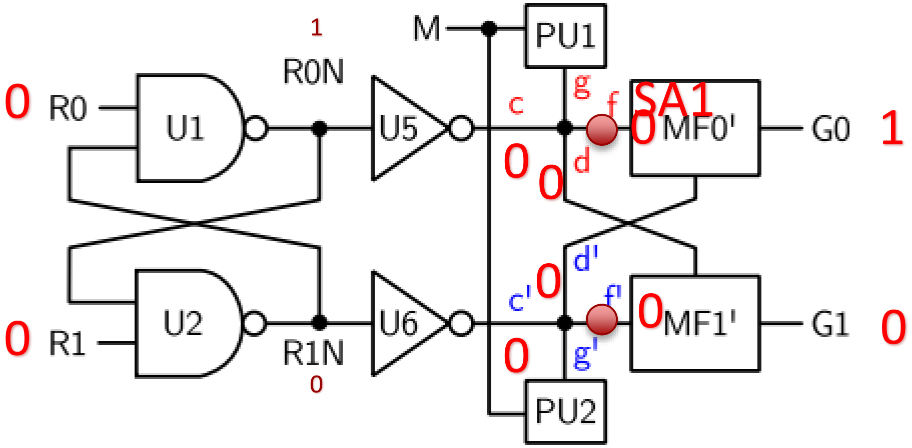
Gate-level Model



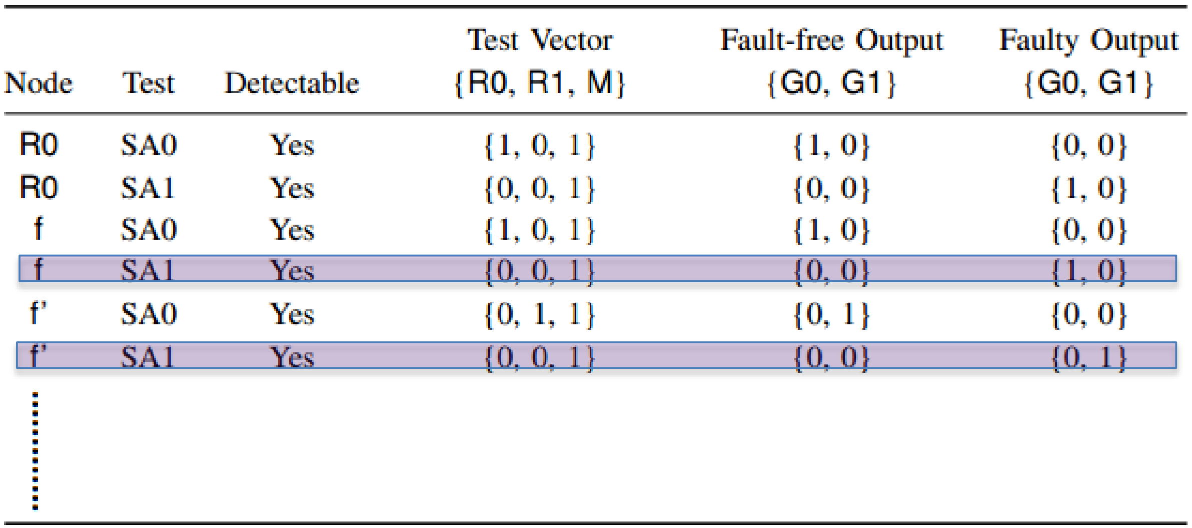
Layout (STM 65nm)

- Two inverters U5 and U6 added
  - Isolates MS nodes
- Two PMOS MP5 and MP6 added
  - Helps test metastability filter
- Forces MS when R0=R1=M=0

Fault Coverage



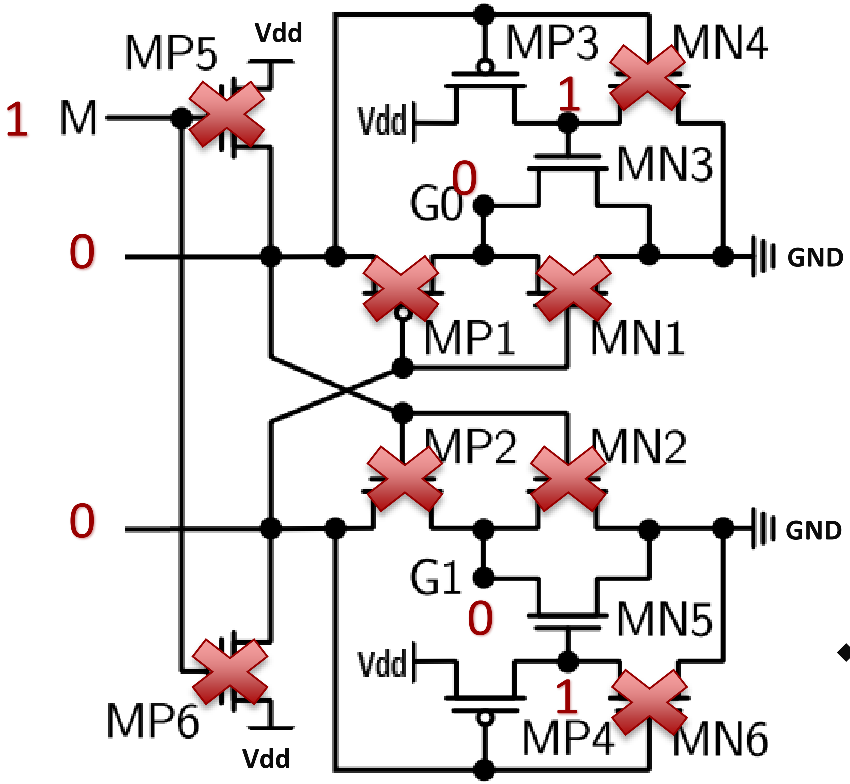
- The marked SA1 faults are undetectable in classic MUTEX
- Now they become testable!



Node	Test	Detectable	Test Vector {R0, R1, M}	Fault-free Output {G0, G1}	Faulty Output {G0, G1}
R0	SA0	Yes	{1, 0, 1}	{1, 0}	{0, 0}
R0	SA1	Yes	{0, 0, 1}	{0, 0}	{1, 0}
f	SA0	Yes	{1, 0, 1}	{1, 0}	{0, 0}
f	SA1	Yes	{0, 0, 1}	{0, 0}	{1, 0}
f'	SA0	Yes	{0, 1, 1}	{0, 1}	{0, 0}
f'	SA1	Yes	{0, 0, 1}	{0, 0}	{0, 1}

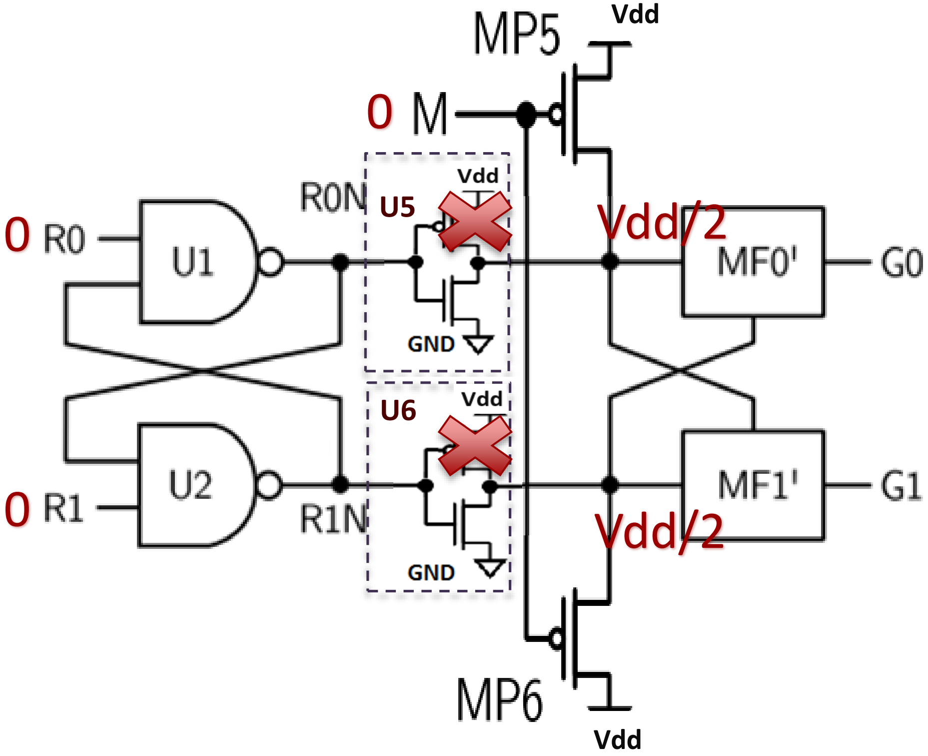
Partial Stuck-At-Fault Analysis

Floating Output Problem and Solution



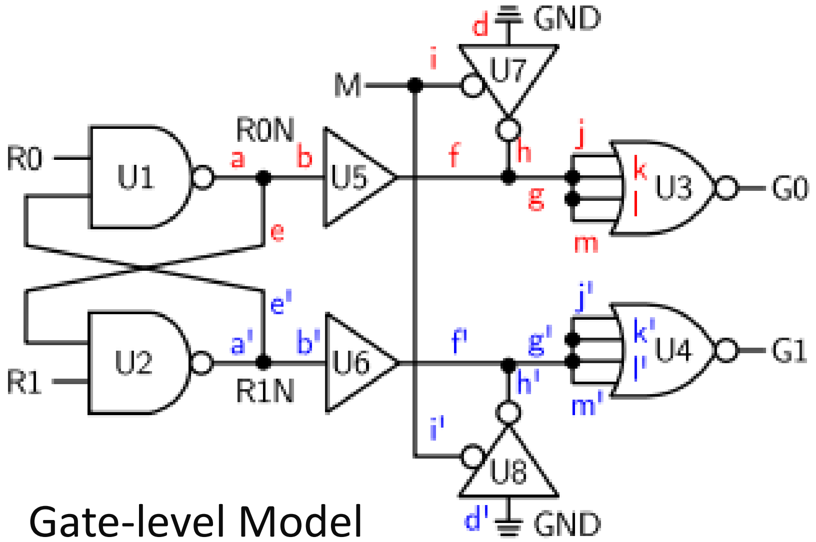
- The Problem: G0 and G1 may float
  - {R0, R1, M} = {0, 0, 1}
  - MF inputs are 0
  - MP1, MN1, MP2, MN2 are in cut-off state
  - G0 and G1 float
- The Solution for floating G0
  - Add MP3, MN3 and MN4
  - Forces a strong 0 on G0
- Same solution for node G1

Testable Metastability Filter

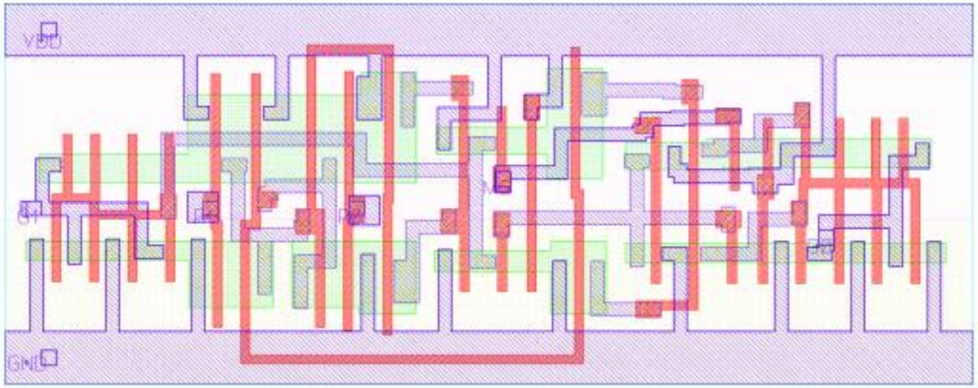


- ❖The input of MS filter is ~Vdd/2 when M = 0 and input of U5 = 1

Proposed Testable MUTEX (Standard-Cell)



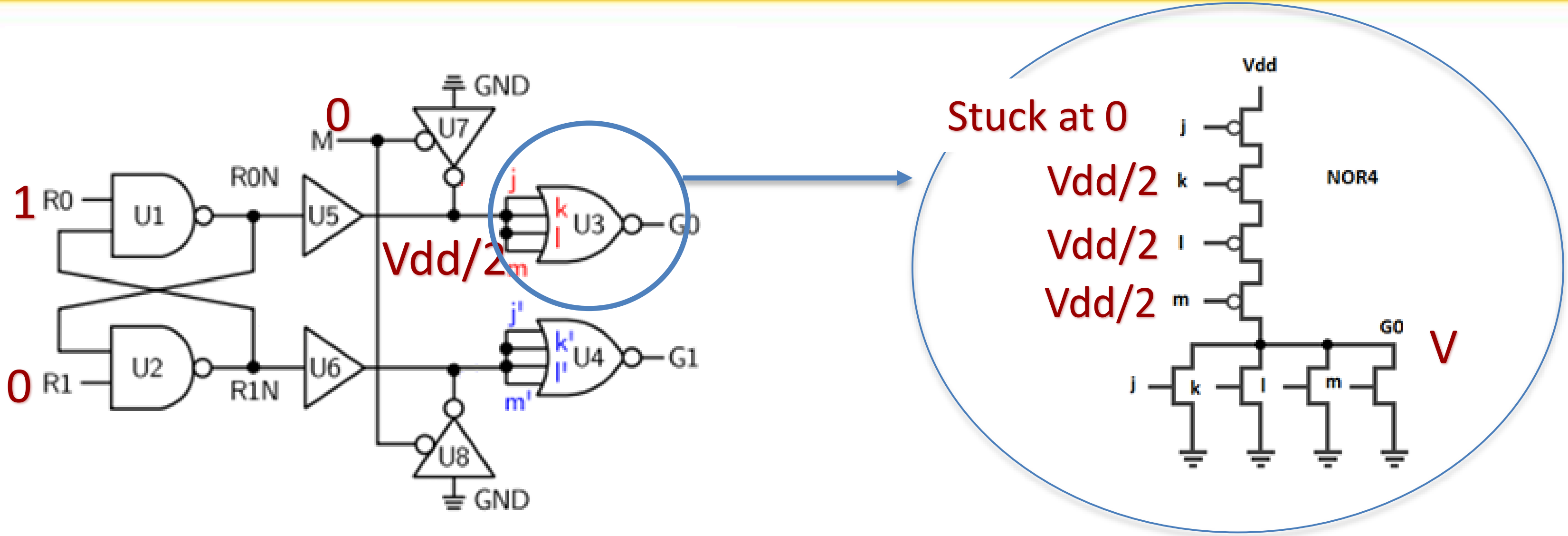
Gate-level Model

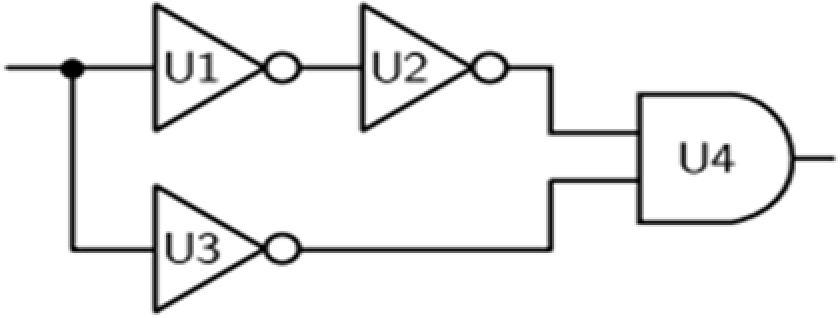


Layout (STM 65nm)

- ❖ Two tri-state inverters U7 and U8 added
  - ❖ Help test metastability filter
- ❖ Two buffers U5 and U6 added
  - ❖ Isolate metastable nodes
  - ❖ Help test metastability filter

Fault Coverage





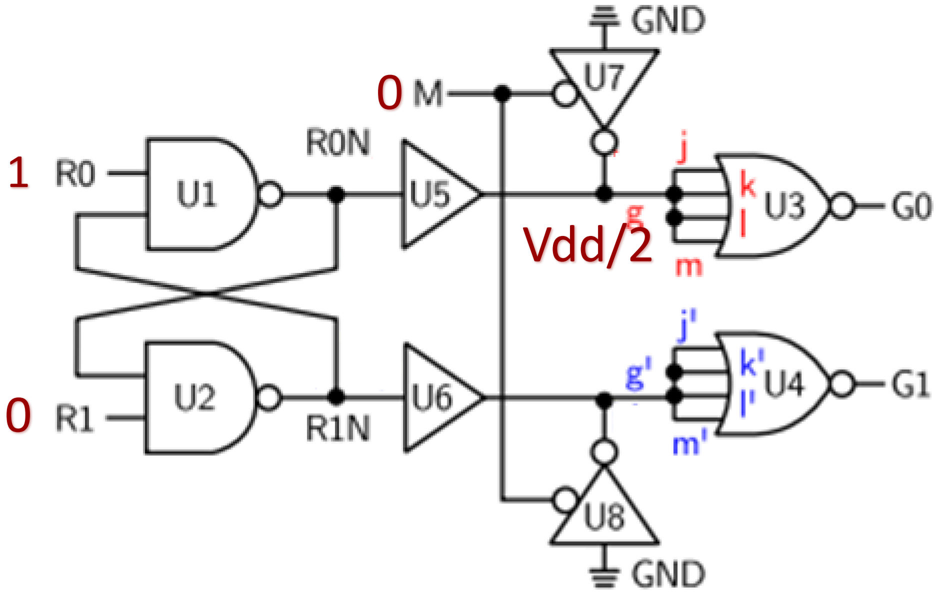
Metastability Detector [Ernst, 2003]

Node	ty Output 0, G1}
R0	0, 0}
R0	1, 0}
i	0, 0}
i	1, 0}
j	V, 0}
j	0, 0}
⋮	

- G0=0 when NOR4 inputs are Vdd/2
- If one of inputs is SA0, voltage of G0 will increase
- May be detected by a metastability detector

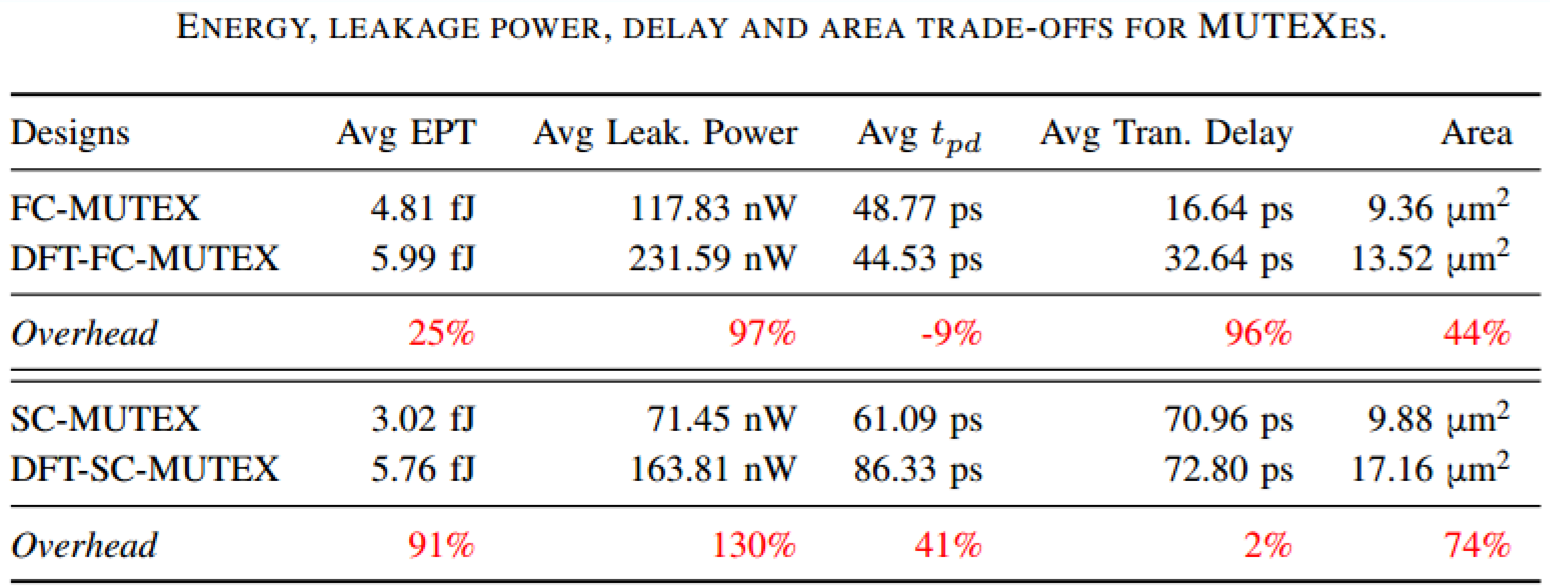
Testable Metastability Filter

Standard Cell
Testable MUTEX



- The input of MS filter (NOR4) is ~Vdd/2 when M=0 and input of U5=0

Experimental Results - Overheads



ENERGY, LEAKAGE POWER, DELAY AND AREA TRADE-OFFS FOR MUTEXES.

Designs	Avg EPT	Avg Leak. Power	Avg t_{pd}	Avg Tran. Delay	Area
FC-MUTEX	4.81 fJ	117.83 nW	48.77 ps	16.64 ps	9.36 μm^2
DFT-FC-MUTEX	5.99 fJ	231.59 nW	44.53 ps	32.64 ps	13.52 μm^2
Overhead	25%	97%	-9%	96%	44%
SC-MUTEX	3.02 fJ	71.45 nW	61.09 ps	70.96 ps	9.88 μm^2
DFT-SC-MUTEX	5.76 fJ	163.81 nW	86.33 ps	72.80 ps	17.16 μm^2
Overhead	91%	130%	41%	2%	74%

- Proposed design introduces overheads because of added transistors
- DFT-FC-MUTEX has a smaller propagation delay than original
- DFT-SC-MUTEX has a larger propagation delay than original

Experimental Results and MTBF Analysis

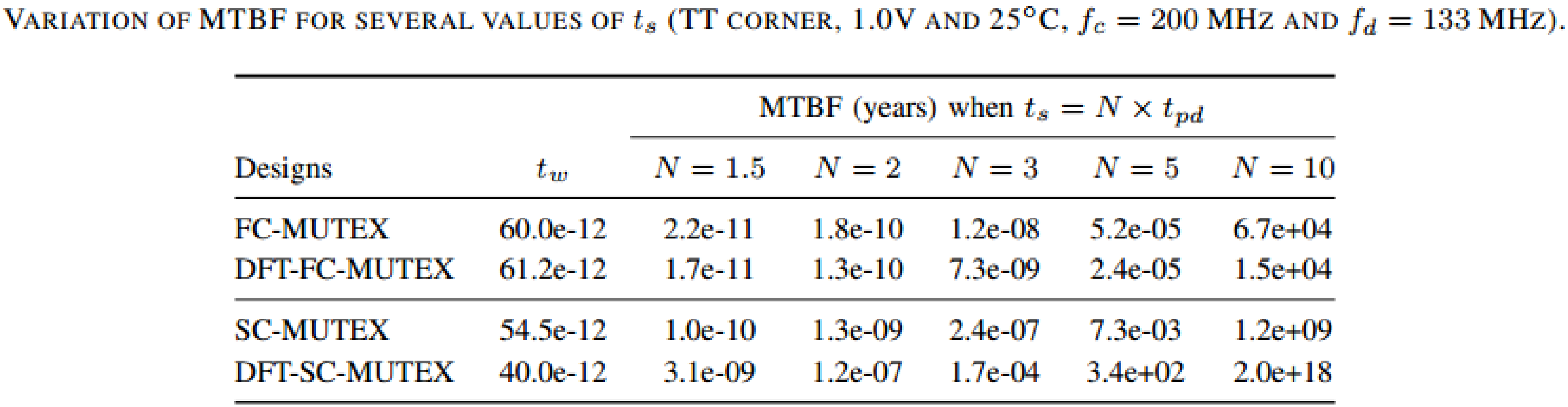
Mean Time Between Failure (MTBF) Analysis

$$MTBF = \frac{e^{t_s/\tau}}{t_w f_c f_d}$$

- τ is the resolution time constant
- t_s is the settling time in which metastability should resolve to a valid logic value
- t_w is the time window during which the MUTEX is vulnerable to metastability
- f_c and f_d are respectively the clock and data rates

Async circuits with MUTEXes typically do not "fail"
but do instantaneously slow down

Experimental Results - MTBF



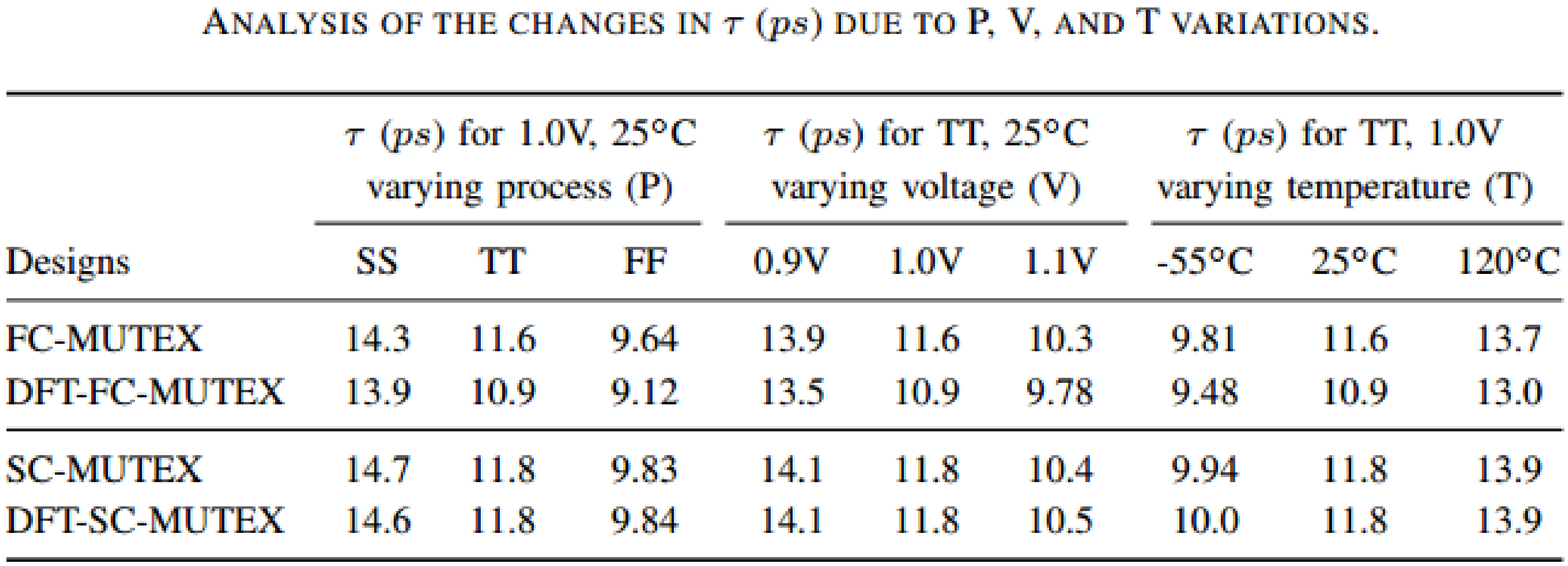
VARIATION OF MTBF FOR SEVERAL VALUES OF t_s (TT CORNER, 1.0V AND 25°C, $f_c = 200$ MHZ AND $f_d = 133$ MHZ).

		MTBF (years) when $t_s = N \times t_{pd}$				
Designs	t_w	$N = 1.5$	$N = 2$	$N = 3$	$N = 5$	$N = 10$
FC-MUTEX	60.0e-12	2.2e-11	1.8e-10	1.2e-08	5.2e-05	6.7e+04
DFT-FC-MUTEX	61.2e-12	1.7e-11	1.3e-10	7.3e-09	2.4e-05	1.5e+04
SC-MUTEX	54.5e-12	1.0e-10	1.3e-09	2.4e-07	7.3e-03	1.2e+09
DFT-SC-MUTEX	40.0e-12	3.1e-09	1.2e-07	1.7e-04	3.4e+02	2.0e+18

- Mean Time Between Failures (MTBF) analyzed using Blendics's MetaAce
- Consider t_s values of 1.5, 2, 3, 5 and 10 times t_{pd}, where t_{pd} is the nominal delay of the MUTEX under analysis

Metastability resolves close to as fast as original MUTEXes

Experimental Results – PVT Analysis



ANALYSIS OF THE CHANGES IN τ (ps) DUE TO P, V, AND T VARIATIONS.

	τ (ps) for 1.0V, 25°C varying process (P)			τ (ps) for TT, 25°C varying voltage (V)			τ (ps) for TT, 1.0V varying temperature (T)		
Designs	SS	TT	FF	0.9V	1.0V	1.1V	-55°C	25°C	120°C
FC-MUTEX	14.3	11.6	9.64	13.9	11.6	10.3	9.81	11.6	13.7
DFT-FC-MUTEX	13.9	10.9	9.12	13.5	10.9	9.78	9.48	10.9	13.0
SC-MUTEX	14.7	11.8	9.83	14.1	11.8	10.4	9.94	11.8	13.9
DFT-SC-MUTEX	14.6	11.8	9.84	14.1	11.8	10.5	10.0	11.8	13.9

The proposed MUTEXes have similar τ values to classic ones, even under PVT variation

Conclusions

- New structures for testable MUTEXes proposed
  - Both full-custom and standard-cell versions
  - Layout created and analyzed

- Key Features
  - Improve fault coverage to 100%
  - Enable testing of Metastability Filters
  - Metastability resolution times not adversely effected

- Performance and power overheads analyzed

Future Work

- Scrutinize impact of **local** PVT variations on MTBF of new MUTEXes
- Tri-state buffers may not be available in all standard-cell libraries
    - Explore alternatives for semi-custom testable MUTEXes
- Test proposed MUTEXes in silicon

Thank You!