ASYNC 2015 – Fresh Ideas

Asynchronous Design for Harsh Environments

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Outline

- Introduction
- Simulation methodology
- Simulation results
- Conclusion and Perspectives

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- **Introduction**
- Simulation methodology
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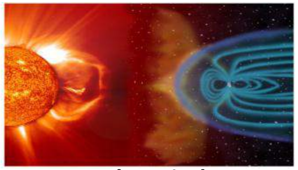
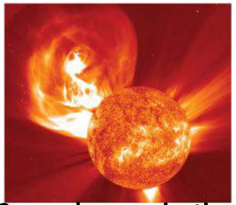
Introduction

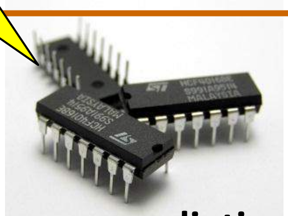
Radiation induced particles


Solar Flare


Solar wind

Energies from keV to 100MeV


Coronal mass ejection



Increase radiation robustness for Non-Volatile circuits

Radiation induced particles

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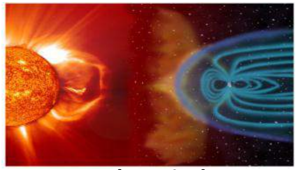

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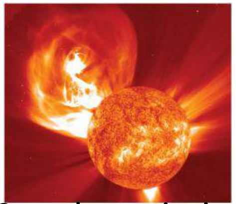
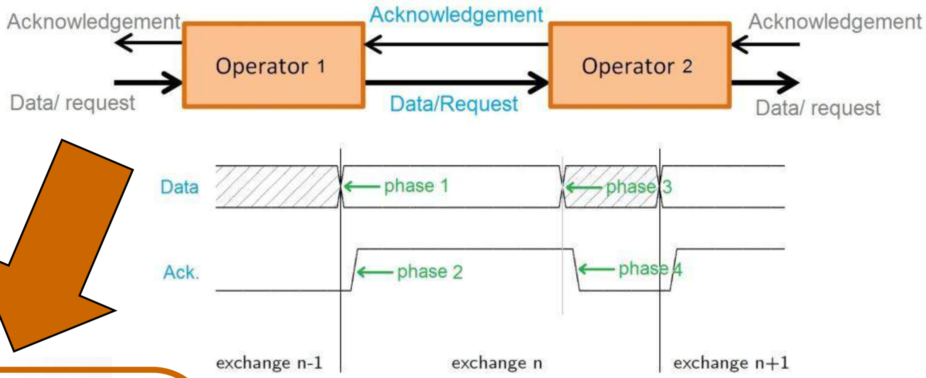
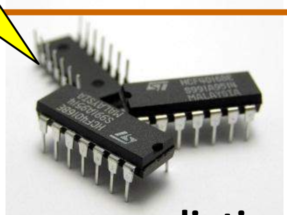


Coronal mass ejection

Asynchronous Communication





Increase radiation robustness for Non-Volatile circuits

Introduction

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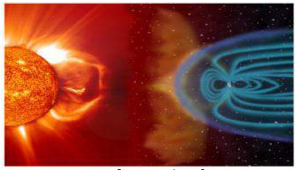

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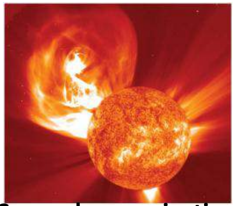

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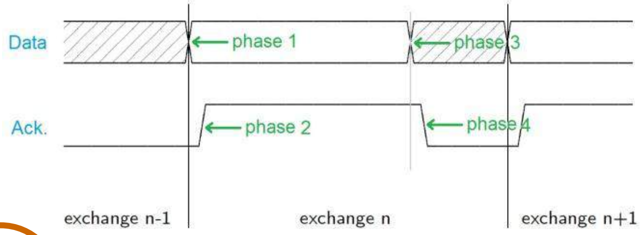
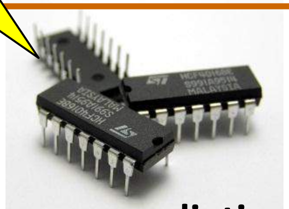
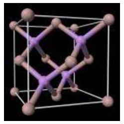
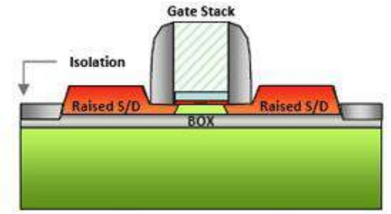




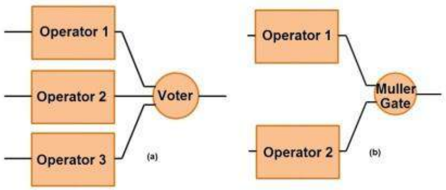
Increase radiation robustness for <u>Non-Volatile</u> circuits

Radiation Hardening Techniques/Process





FD-SOI Device



Philippe Roche, SOI to the rescue

Radiation induced particles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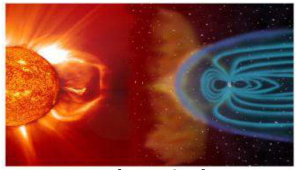
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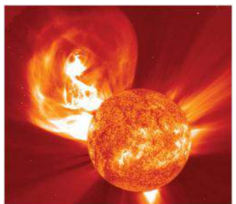
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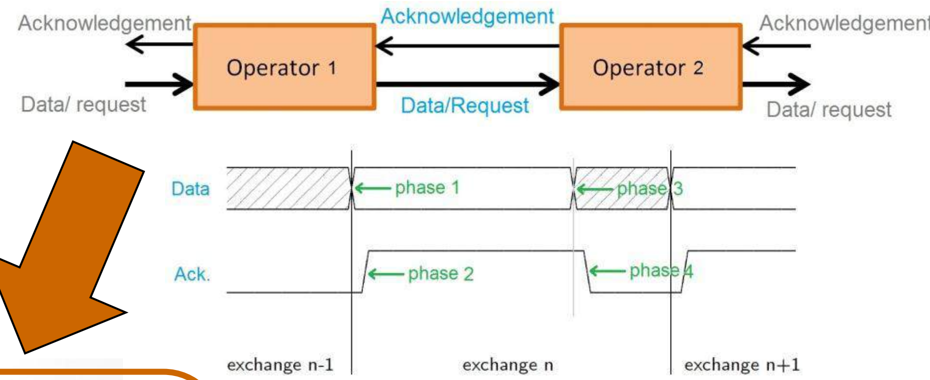
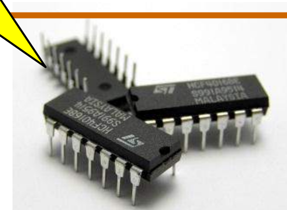
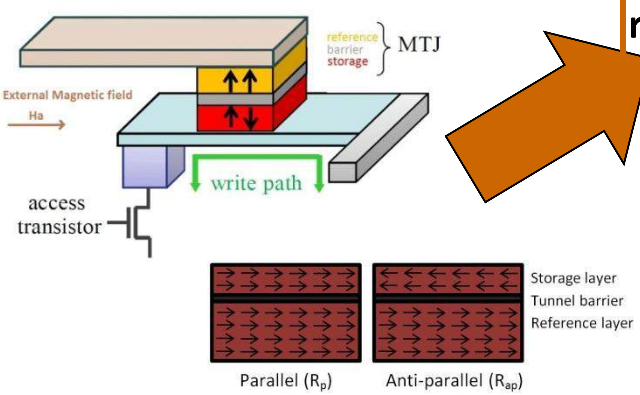




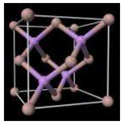
Increase radiation robustness for <u>Non-Volatile</u> circuits

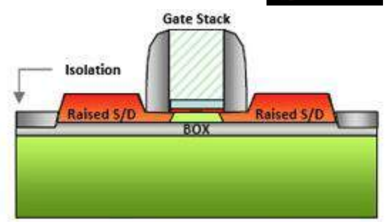
Non-Volatile Memory



Harold Hughes, Radiation studies of spin-transfer torque materials and devices

Radiation Hardening Techniques/Process





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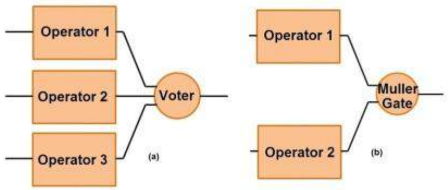

Philippe Roche, SOI to the rescue

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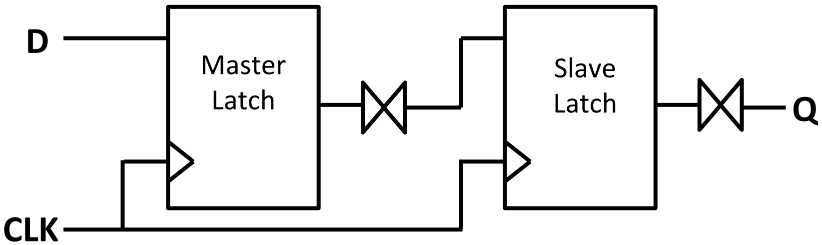
Synchronous

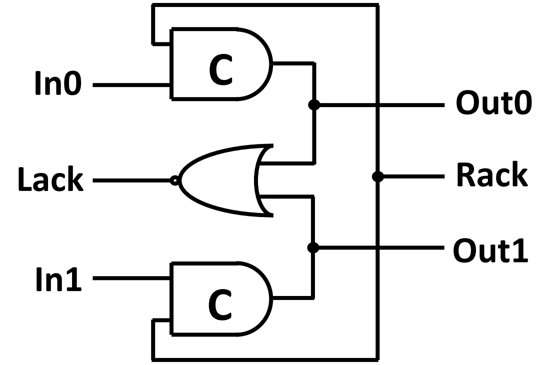
Flip-Flop = Master latch & Slave latch



- 26 transistors
- 15 sensitive nodes

Asynchronous

Half-Buffer = 2 Muller cells & 1 logic gate

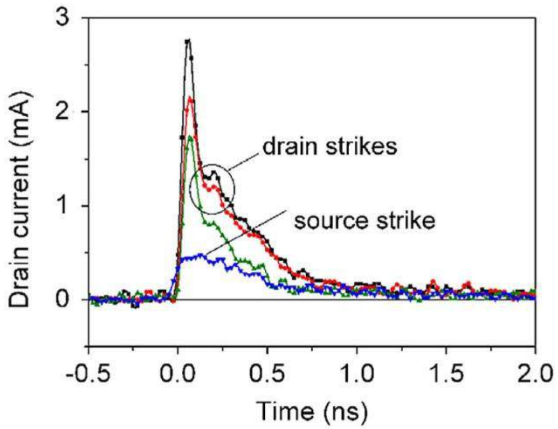


- 28 transistors
- 14 sensitive nodes

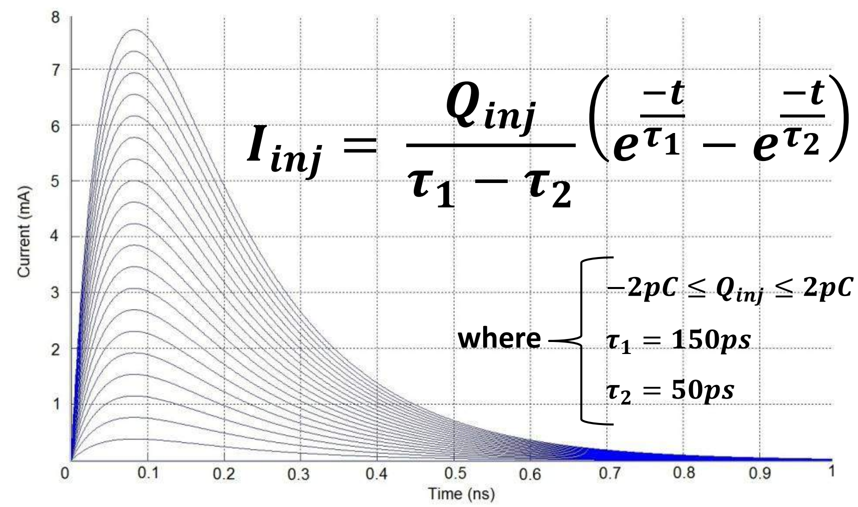
- **Identical timing through transistor sizing**

Circuit type	Number of Errors
Flip-Flop	0.41
NV STT Flip-Flop	0.47
NV SOT Flip-Flop	0.43
Half-Buffer	0.35
NV STT Half-Buffer	0.82
NV SOT Half-Buffer	0.66

Simulation methodology: Particle injection

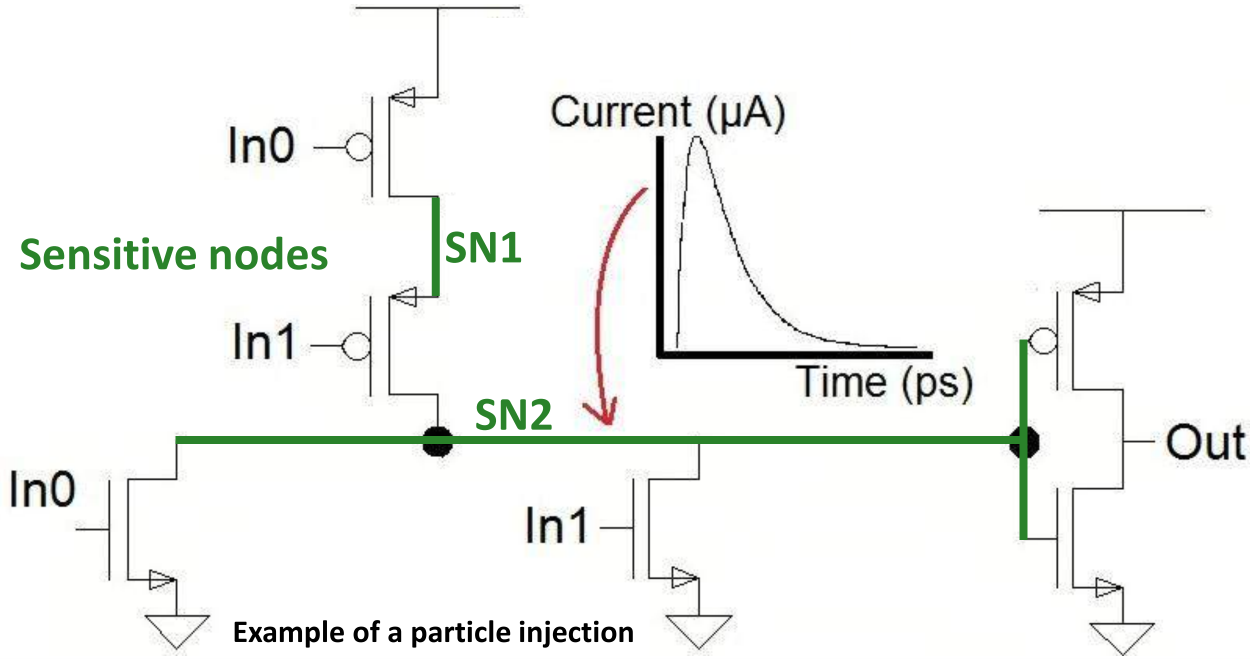


Ferlet-Cavrois, V and Paillet, P and Gaillardin, and others, *Statistical analysis of the charge collected in SOI and bulk devices under heavy Ion and proton irradiation implications for digital SETs*, Nuclear Science, IEEE Transactions on, 2006, vol. 53, no 6, pp. 3242-3252.



$$I_{inj} = \frac{Q_{inj}}{\tau_1 - \tau_2}\left(e^{\frac{-t}{\tau_1}} - e^{\frac{-t}{\tau_2}}\right)$$

where $-2pC \leq Q_{inj} \leq 2pC$, $\tau_1 = 150ps$, $\tau_2 = 50ps$



Example of a particle injection

$Q_{inj} = 470fC$

$I_{inj} = 1,8mA$

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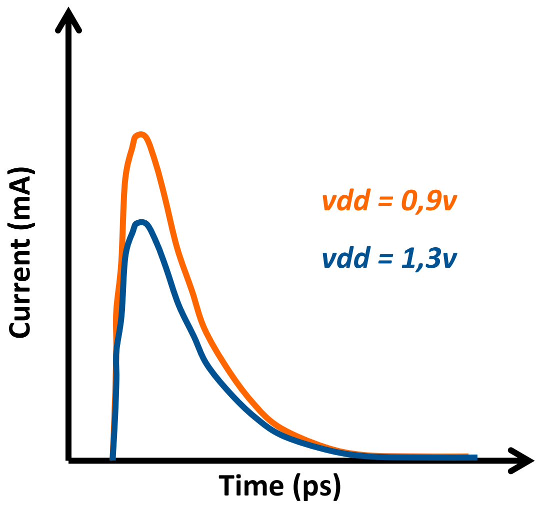
Observations:

As the supply voltage increases, the amplitude of the induced pulse decreases.



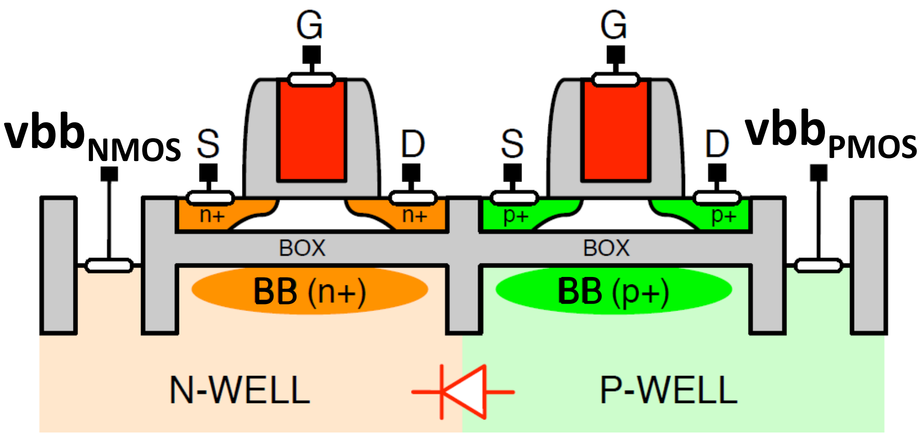
Explanation:

As the supply voltage increases the conductance of the transistors increases also.

Conclusion:

Use the highest supply voltage permitted by the technology for increasing the robustness toward radiation.

Simulation results: Impact of the threshold voltage



Observations:

LVT transistors are more robust than RVT transistors.

Explanation:

LVT transistors have a higher leakage than RVT, so the induced current pulses are evacuated quicker due to the lower resistance.

Conclusion:

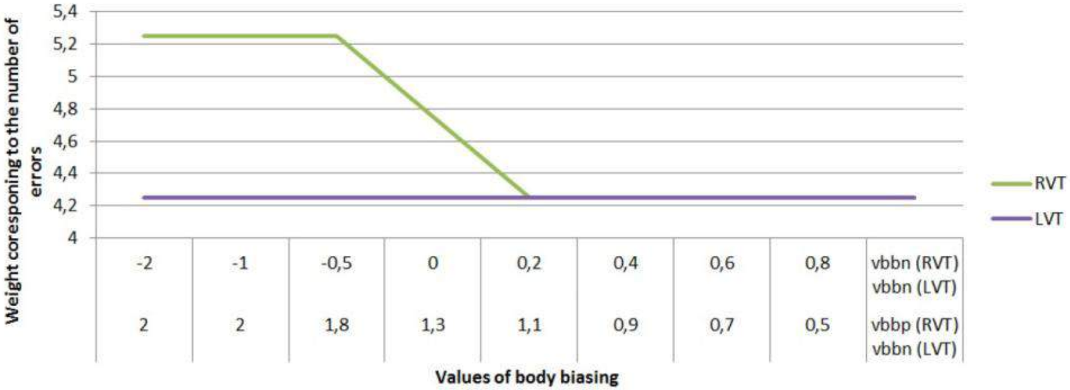
Use LVT transistors for space applications.

Simulation results: Influence of body biasing

Observations:

<u>RVT transistors</u>: The number of errors decreased as vbb increased.

<u>LVT transistors</u>: vbb has no effect on the number of errors.



Explanation:

As vbb increases in RVT transistors , there response is boosted and the accumulated charges caused by particle strikes can be evacuated quicker.

LVT already have a low *vt* so the accumulated *vt* can be evacuated quicker.

Conclusion:

Body biasing has no effect on hardening when using LVT transistors.

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Conclusion and Perspectives

$$Total\ Number\ of\ simulations\ \approx 2000$$

$$(Number\ of\ input\ combinations\ \times Number\ of\ Sensitive\ Nodes\ \times 2 = Number\ of\ simulations)$$

The simulation results have demonstrated that using the highest supply voltage permitted by the technology, in conjunction with LVT transistors is the best option to harden systems at transistor level.

Next Steps:

- **Comparison of Synchronous and Asynchronous architectures in a pipeline**
- **Integration of MTJs in both Synchronous and Asynchronous**
- **Hardening by design (TMR, DMR)**
- **Architecture level studies**

Thank you for your attention !

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