

A reconfigurable device for GALS systems

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Backgrounds

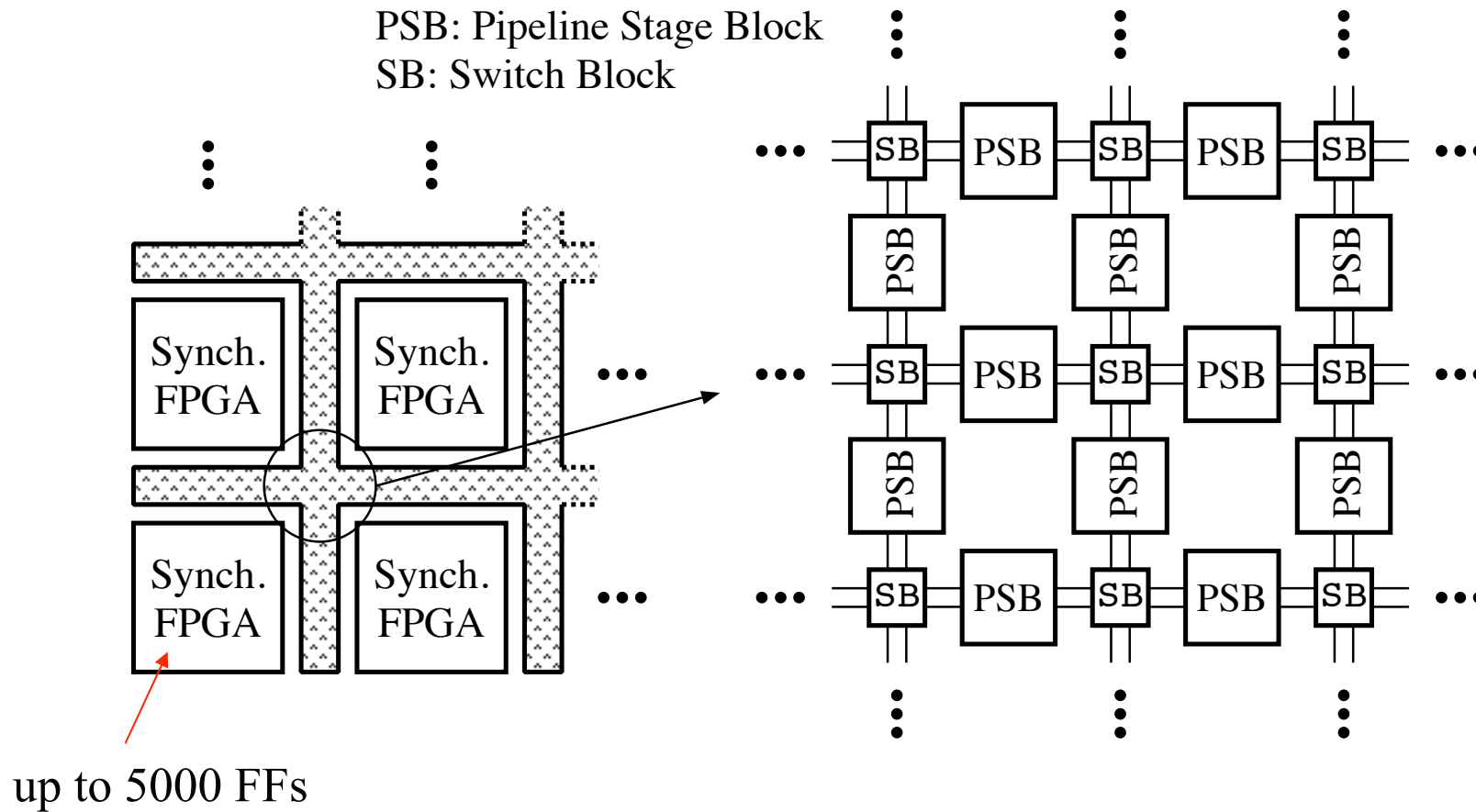
- ◆ FPGAs are now used in many applications
 - not only for prototyping, but also for final products
- ◆ It is not easy to implement large circuits on a large FPGA
 - mainly due to complicated timing constraints
 - GALS approach can be a solution
- ◆ Related work
 - GALS FPGAs
 - Communication mechanism is fixed
 - Asynchronous FPGAs
 - Fine grain architecture, not suitable for GALS approach

Proposed Idea

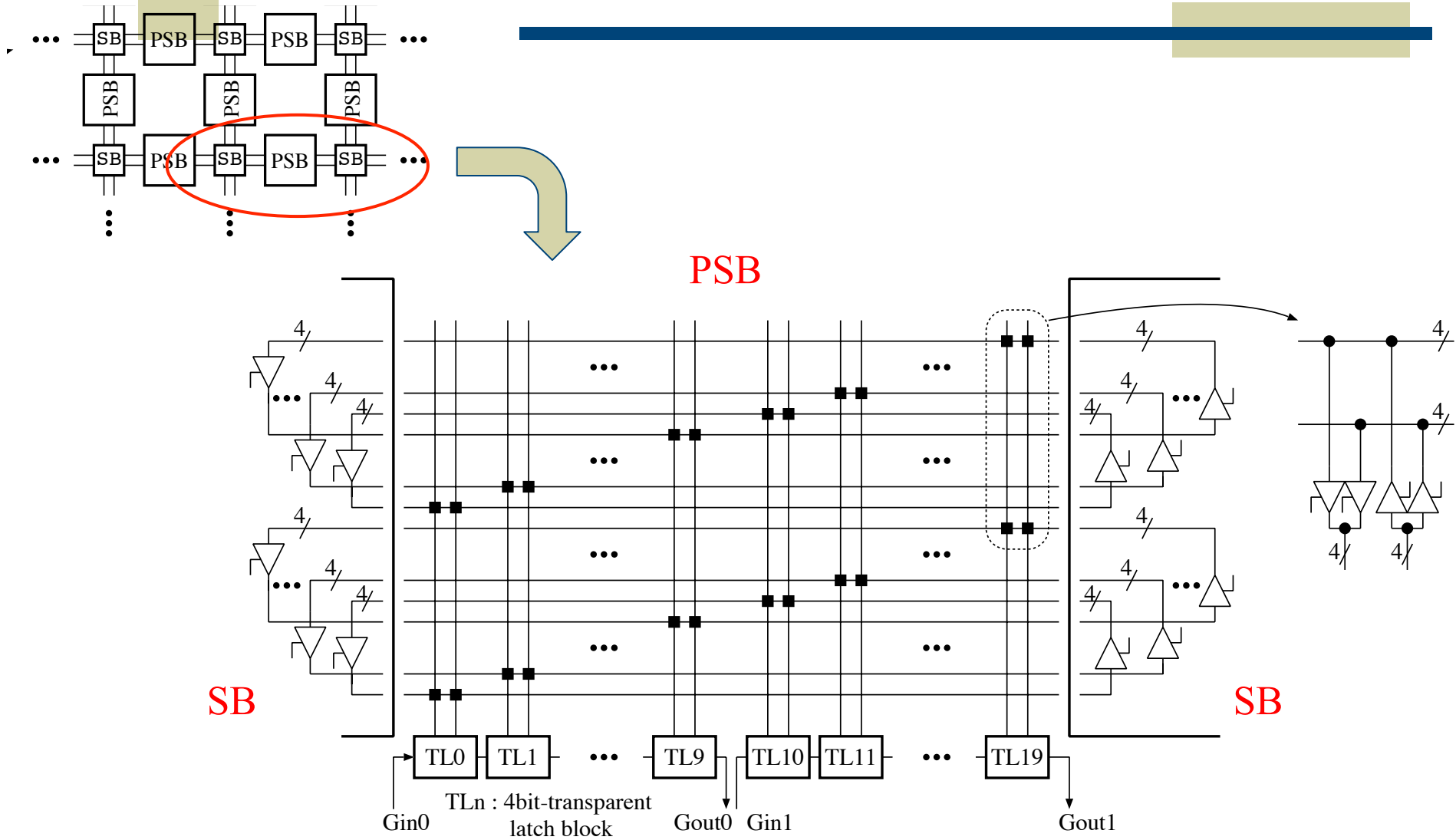
◆ Architecture

- Reconfigurable asynchronous components
 - Specific to communication mechanism
 - ◆ Various functions implementable
 - Routing algorithms
 - Dependability functions
 - Data stream processing, etc.
- Much coarser element blocks
 - Based on MOUSETRAP pipeline stages
 - ◆ Bundled-data style and transition signaling protocol
 - Low power and low performance overhead expected

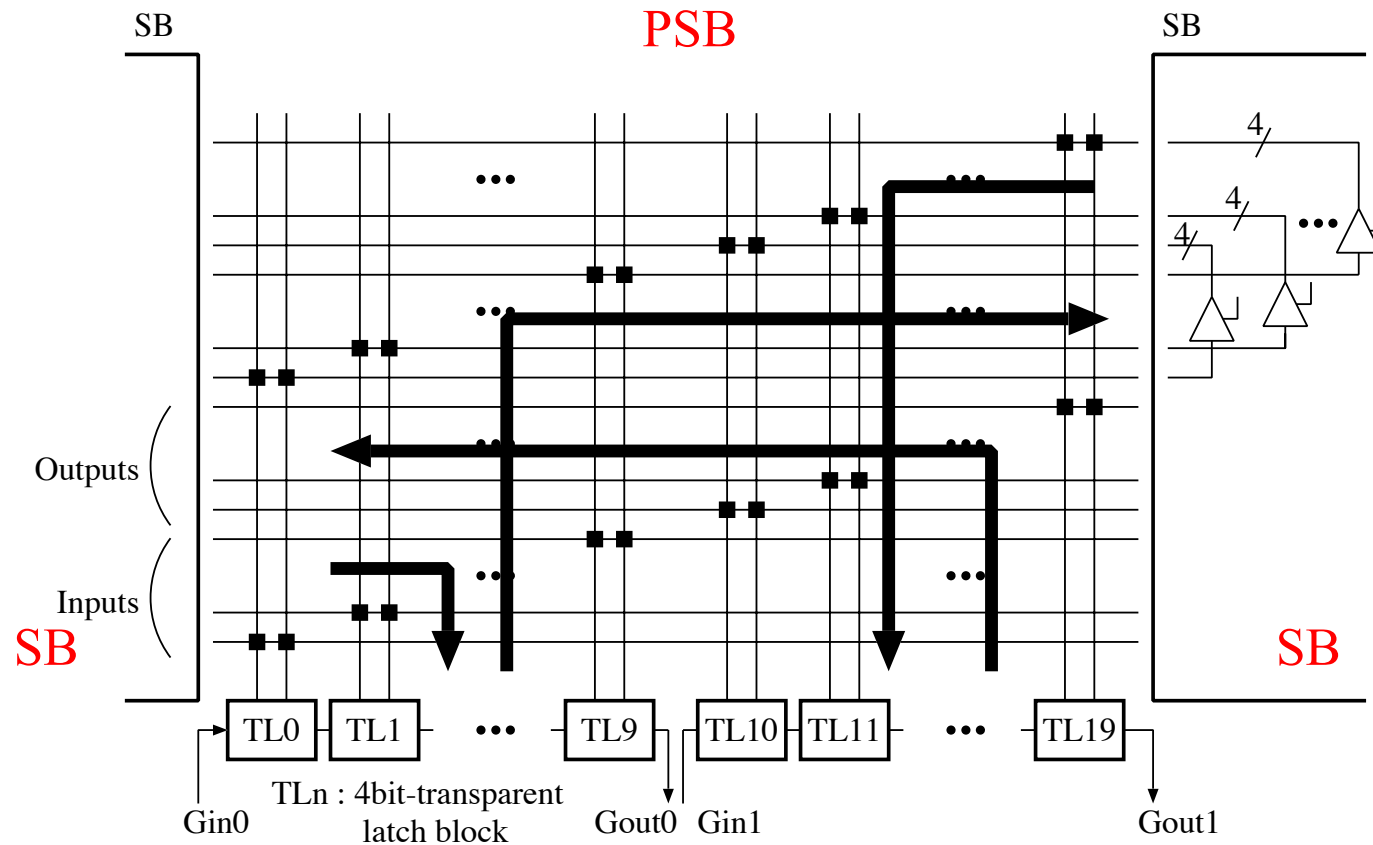
Proposed Architecture



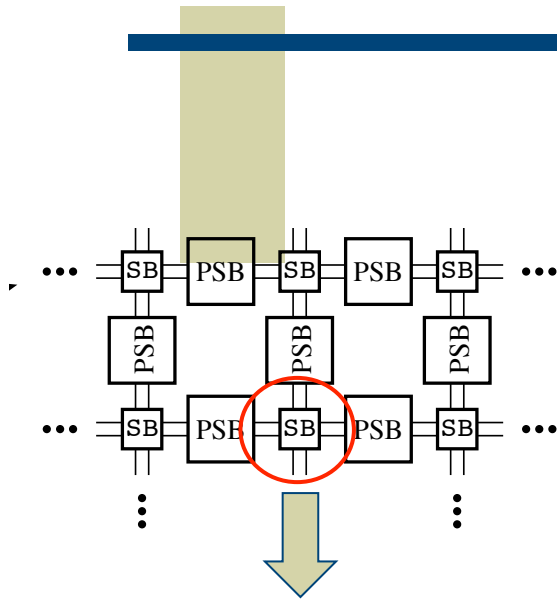
Data-path of PSB



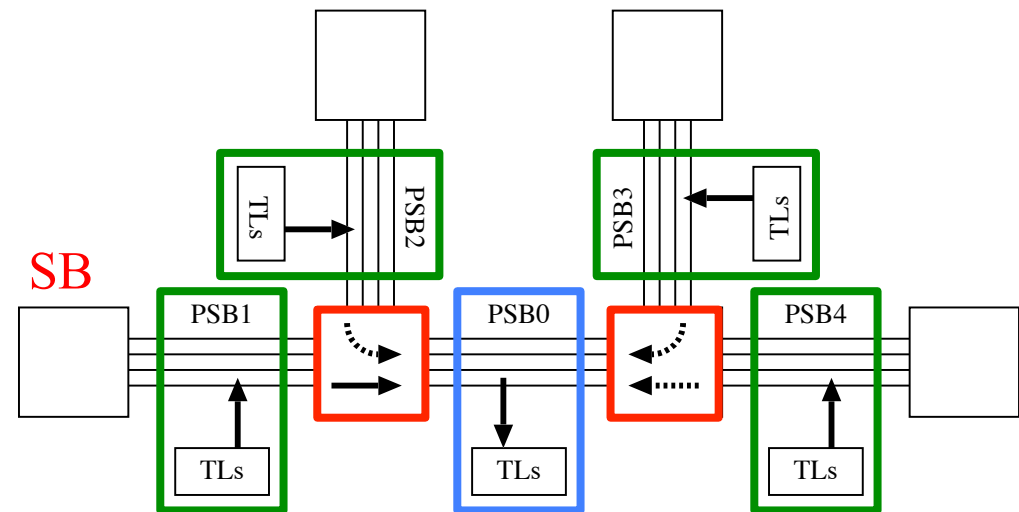
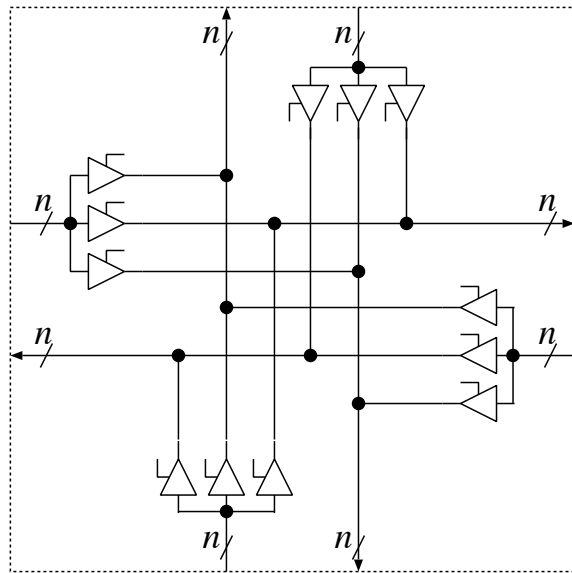
Example of PSB usage



SB (Switch Block)

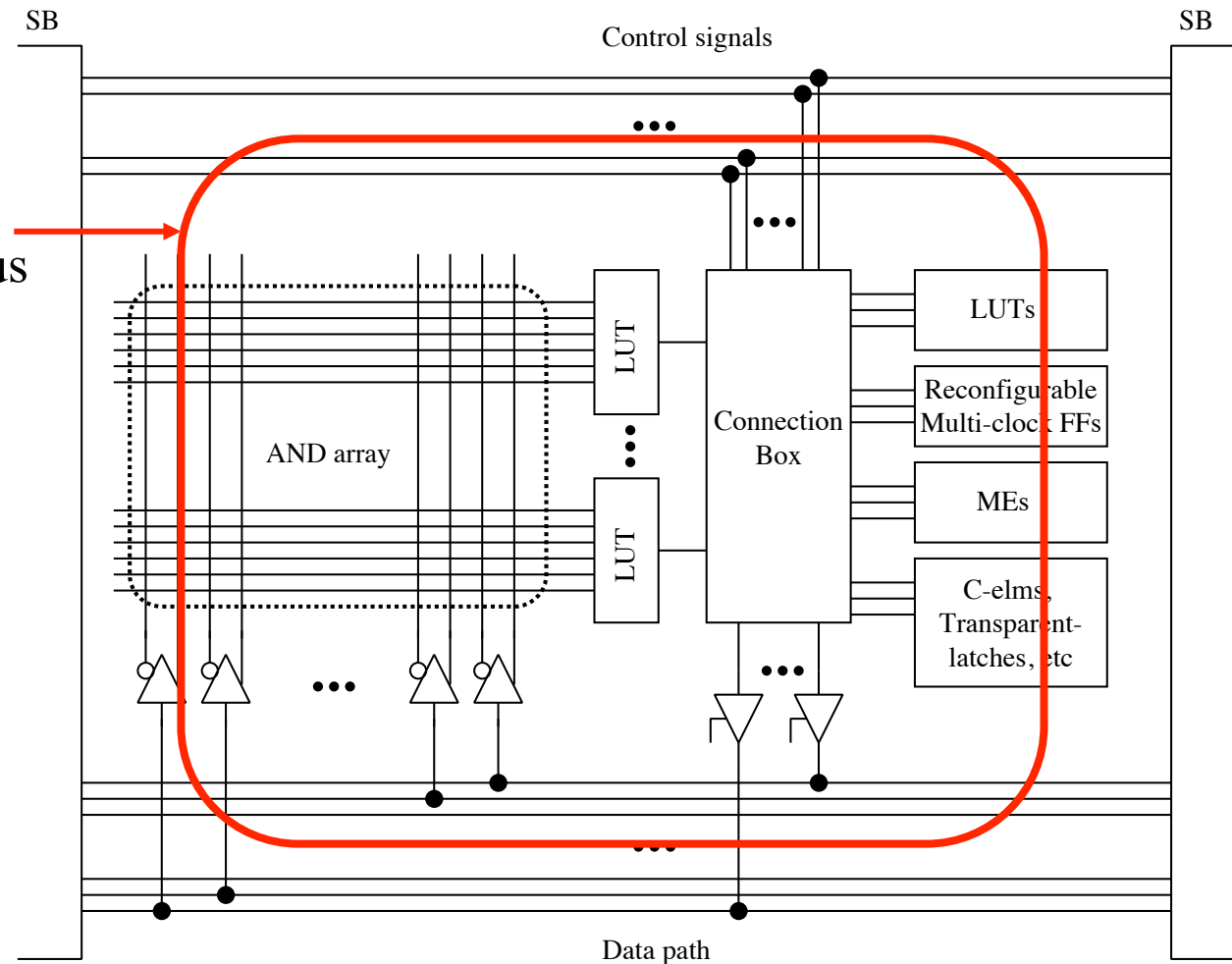


SB

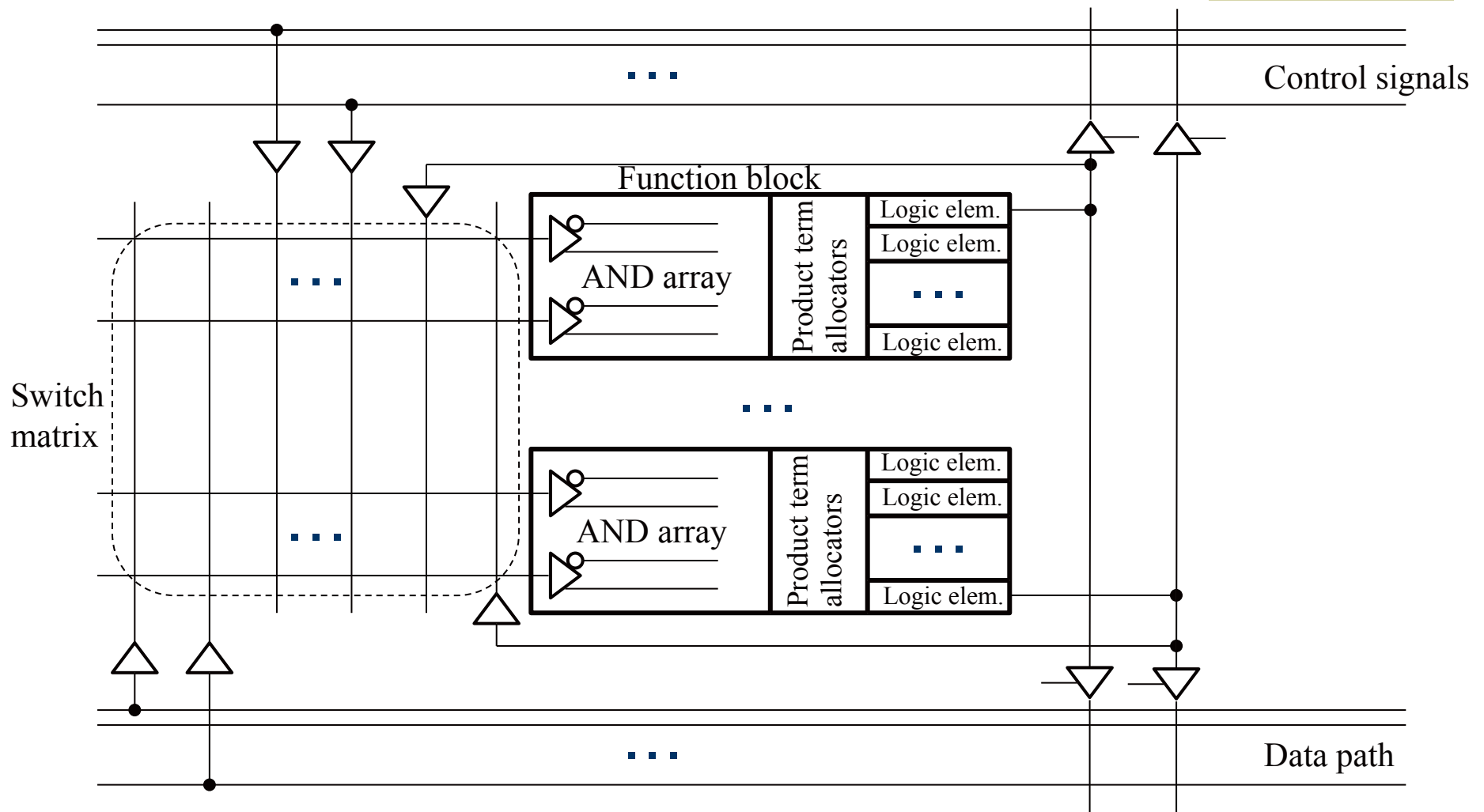


Control circuit in PSB

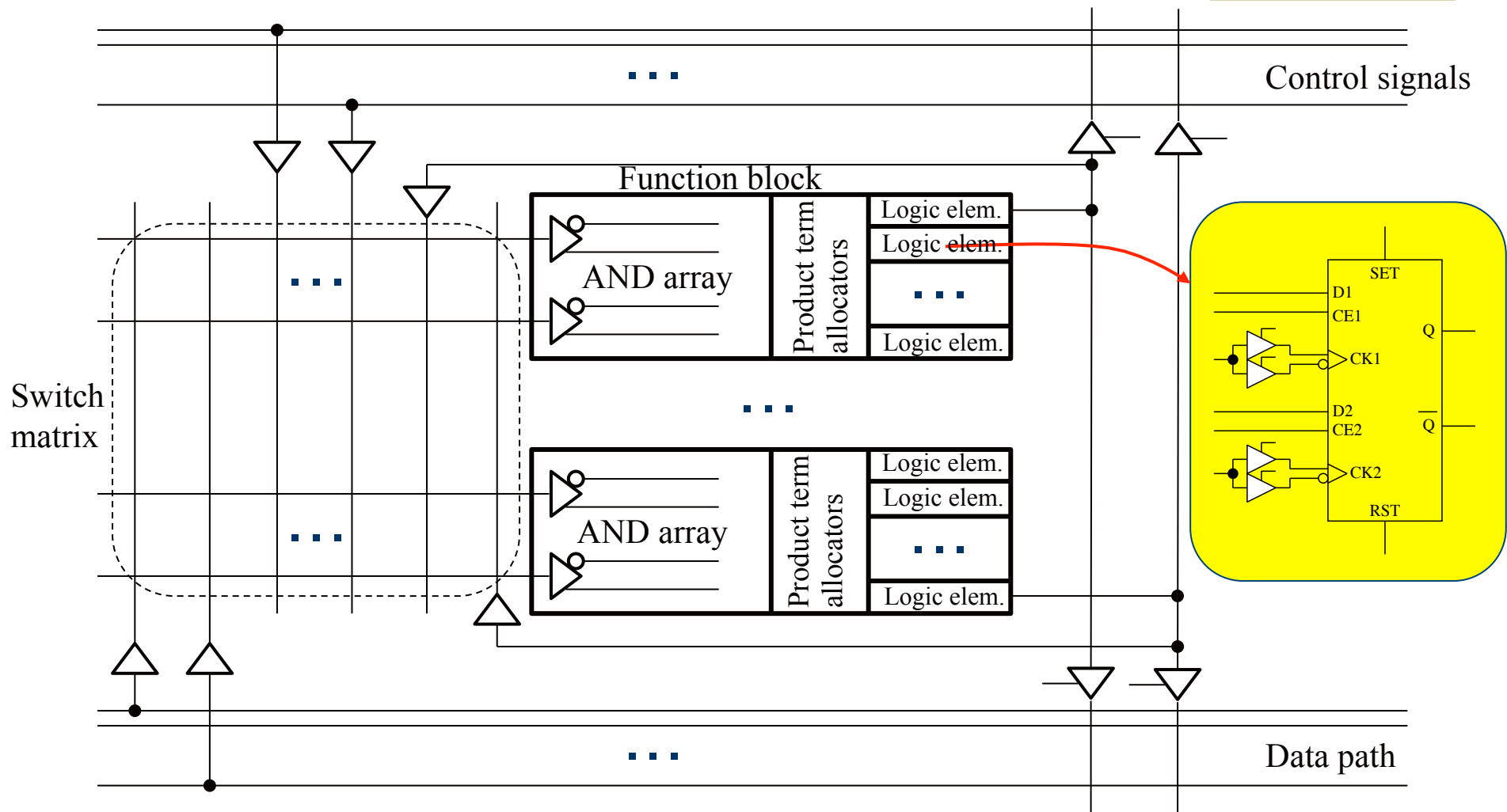
Similar to a small CPLD with various asynchronous cells



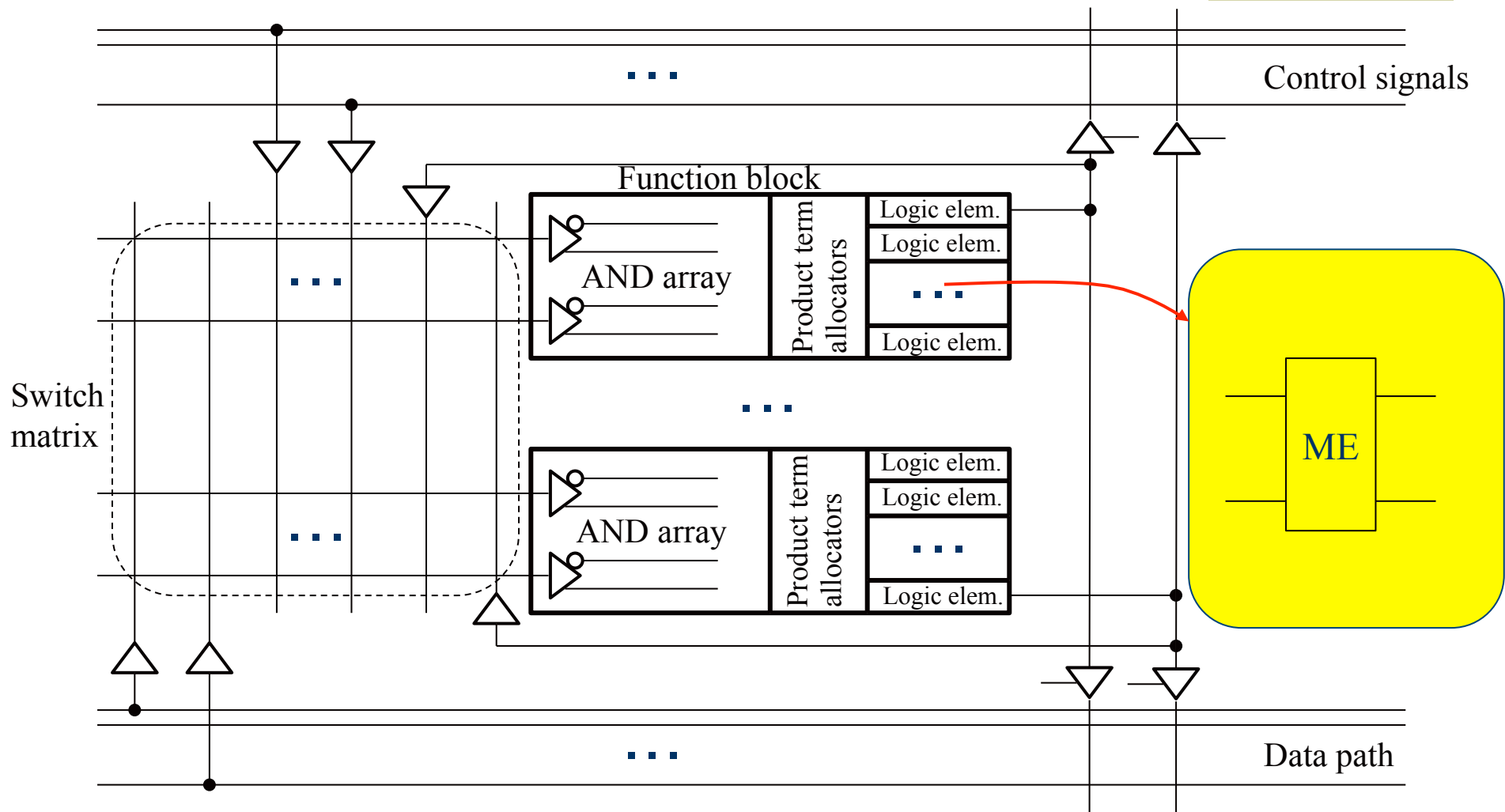
Control circuit in PSB



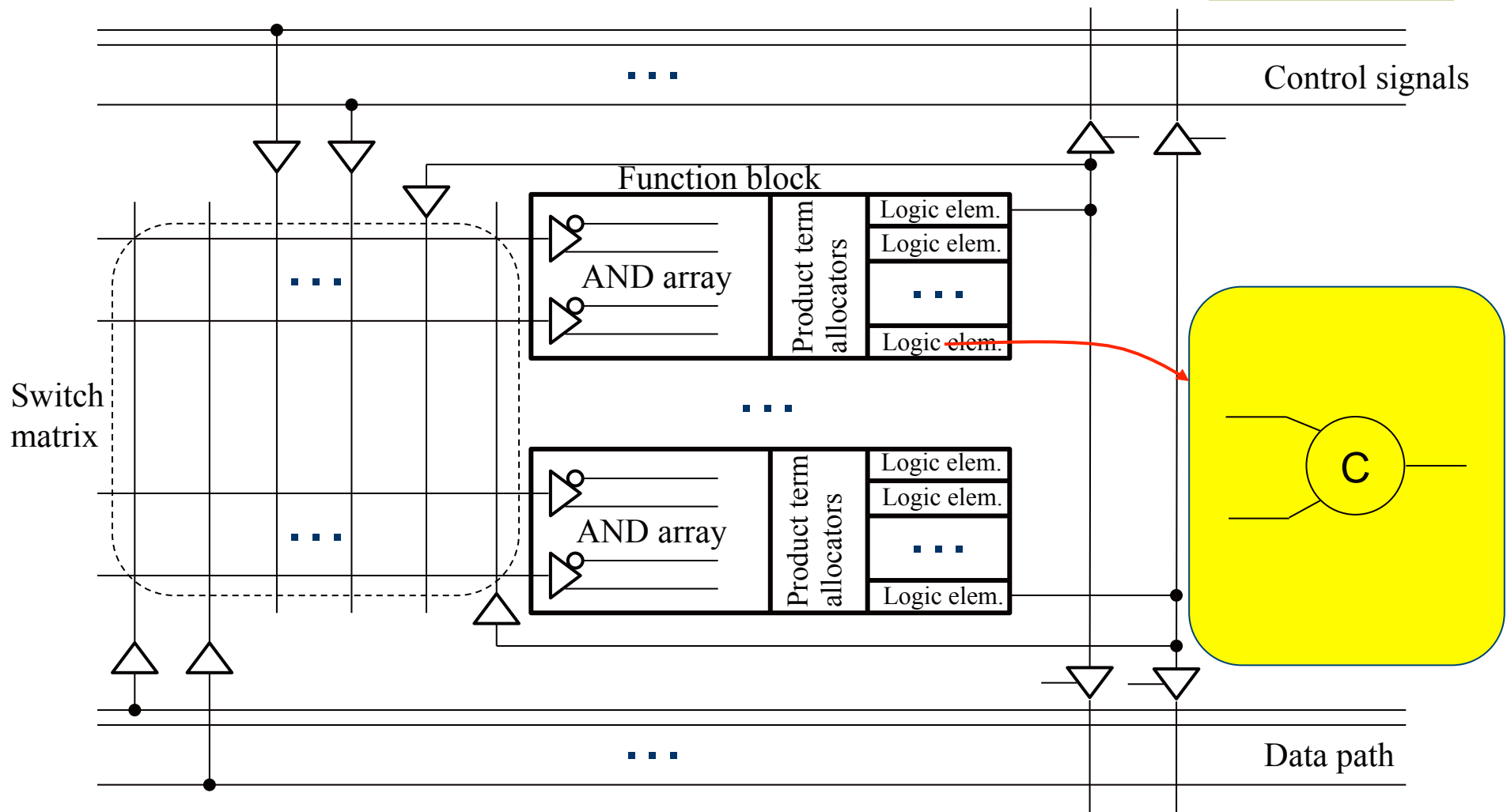
Control circuit in PSB



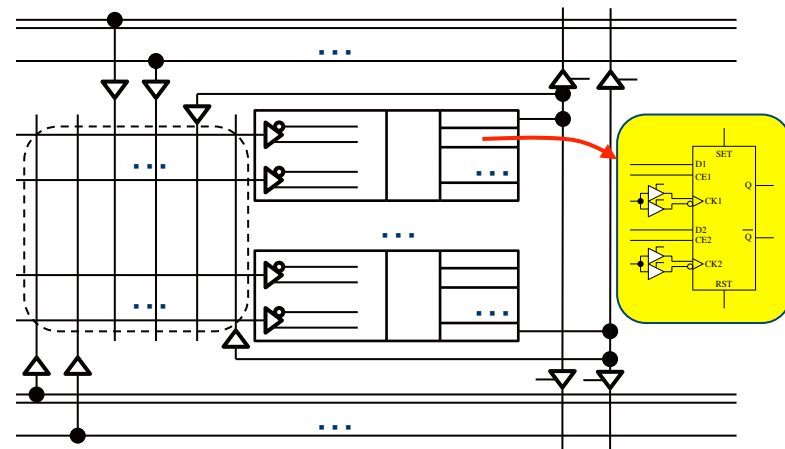
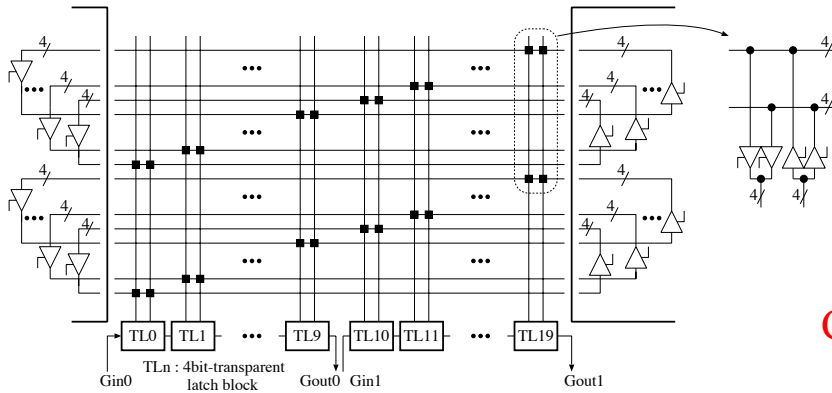
Control circuit in PSB



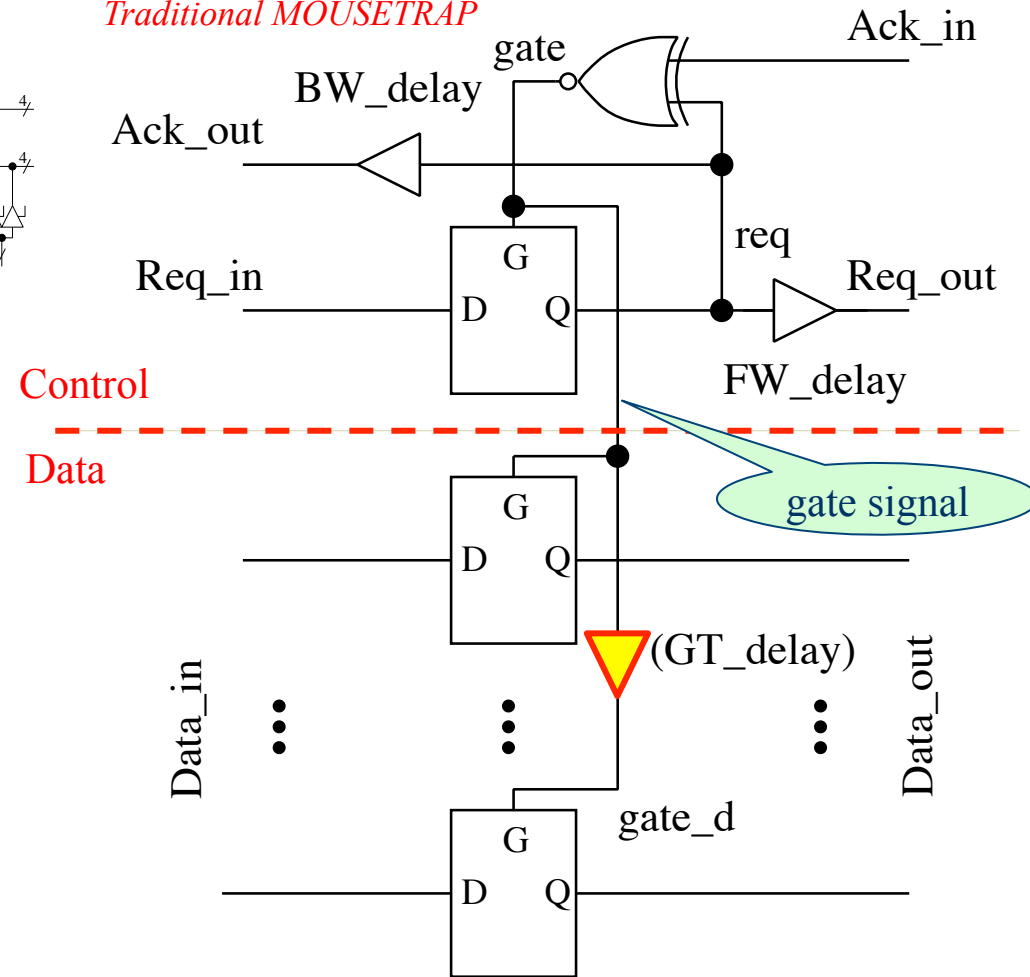
Control circuit in PSB



Delay issue in MOUSETRAP

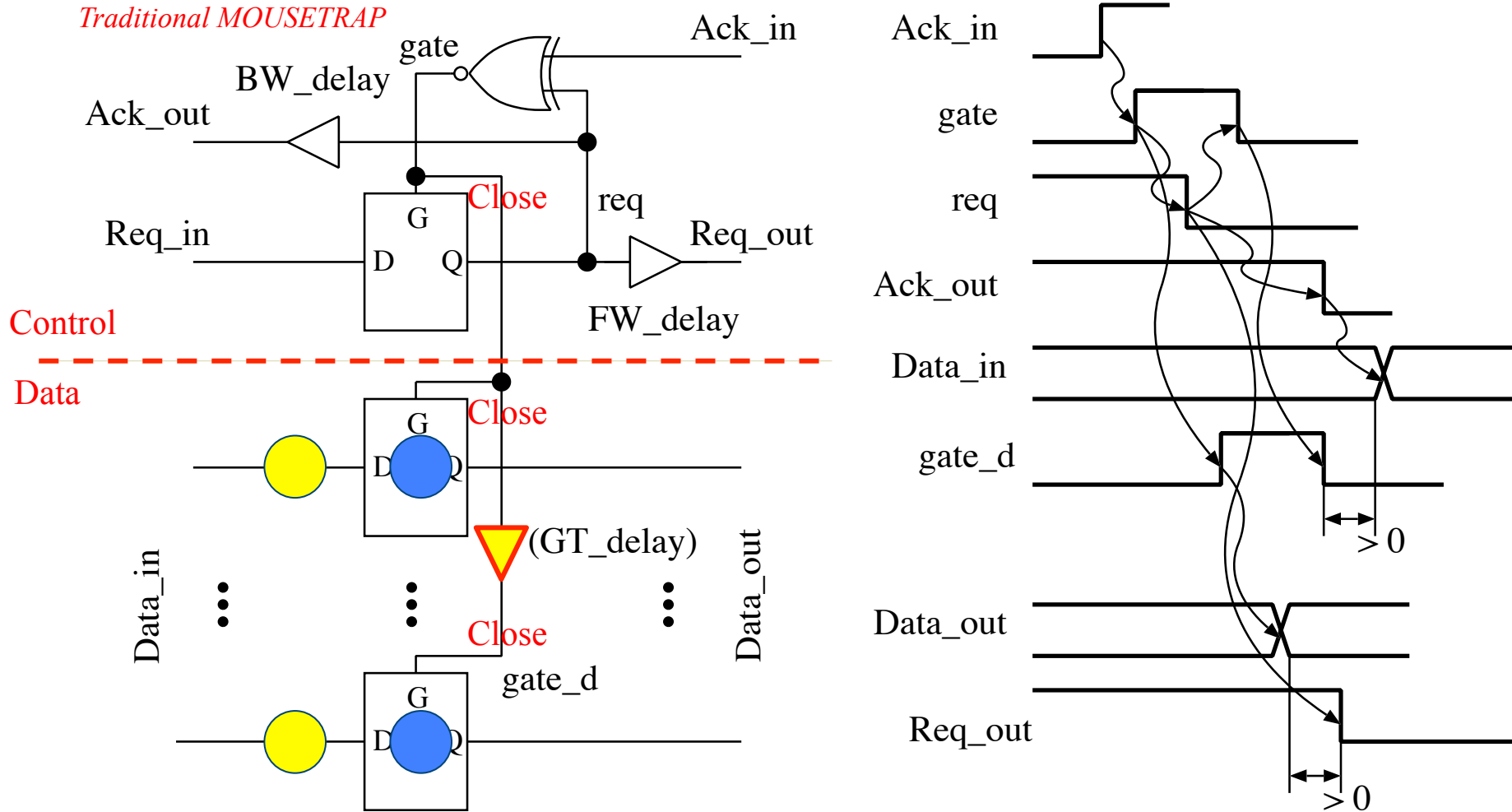


Traditional MOUSETRAP

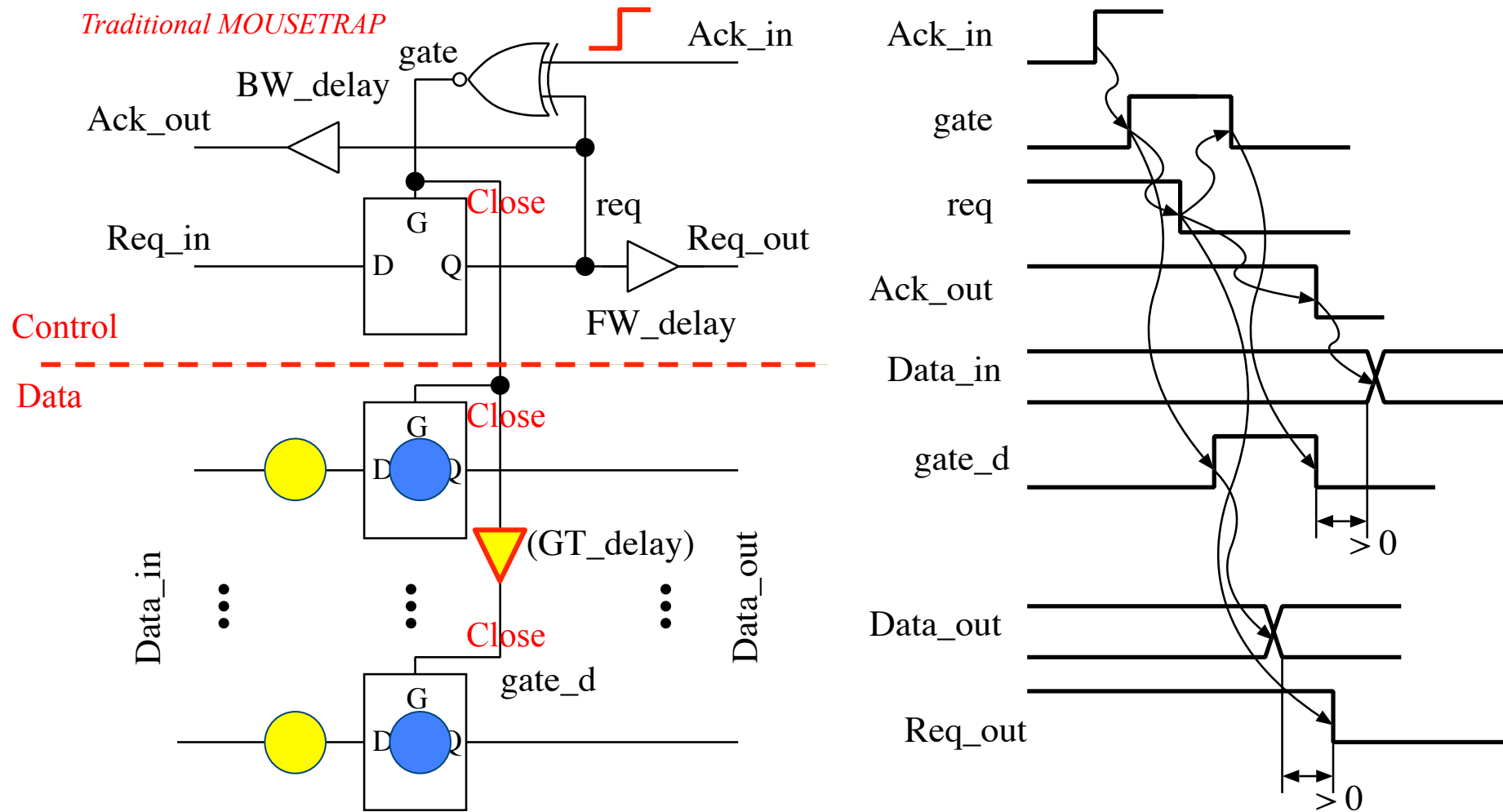


Delay issue in MOUSETRAP

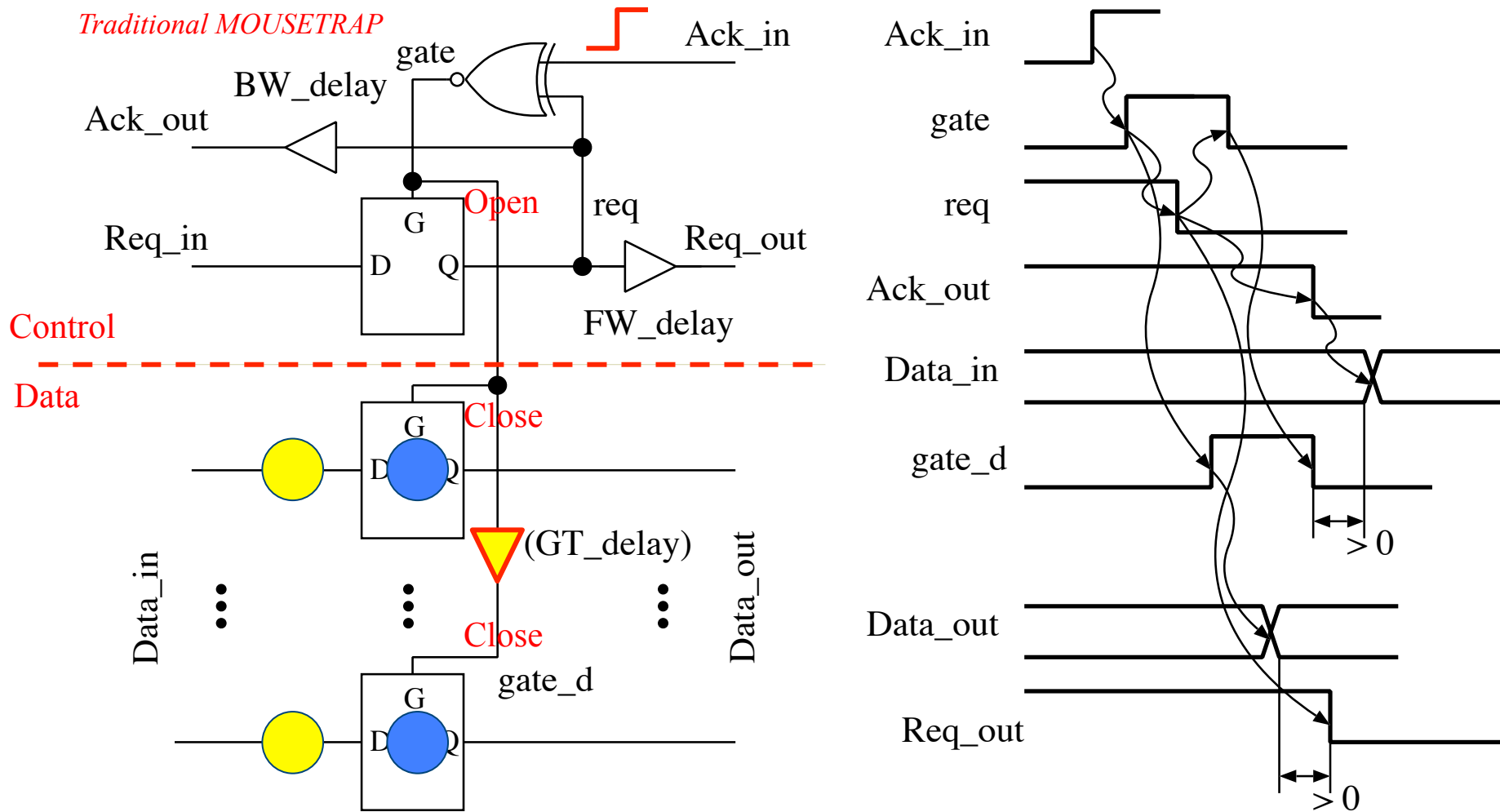
Traditional MOUSETRAP



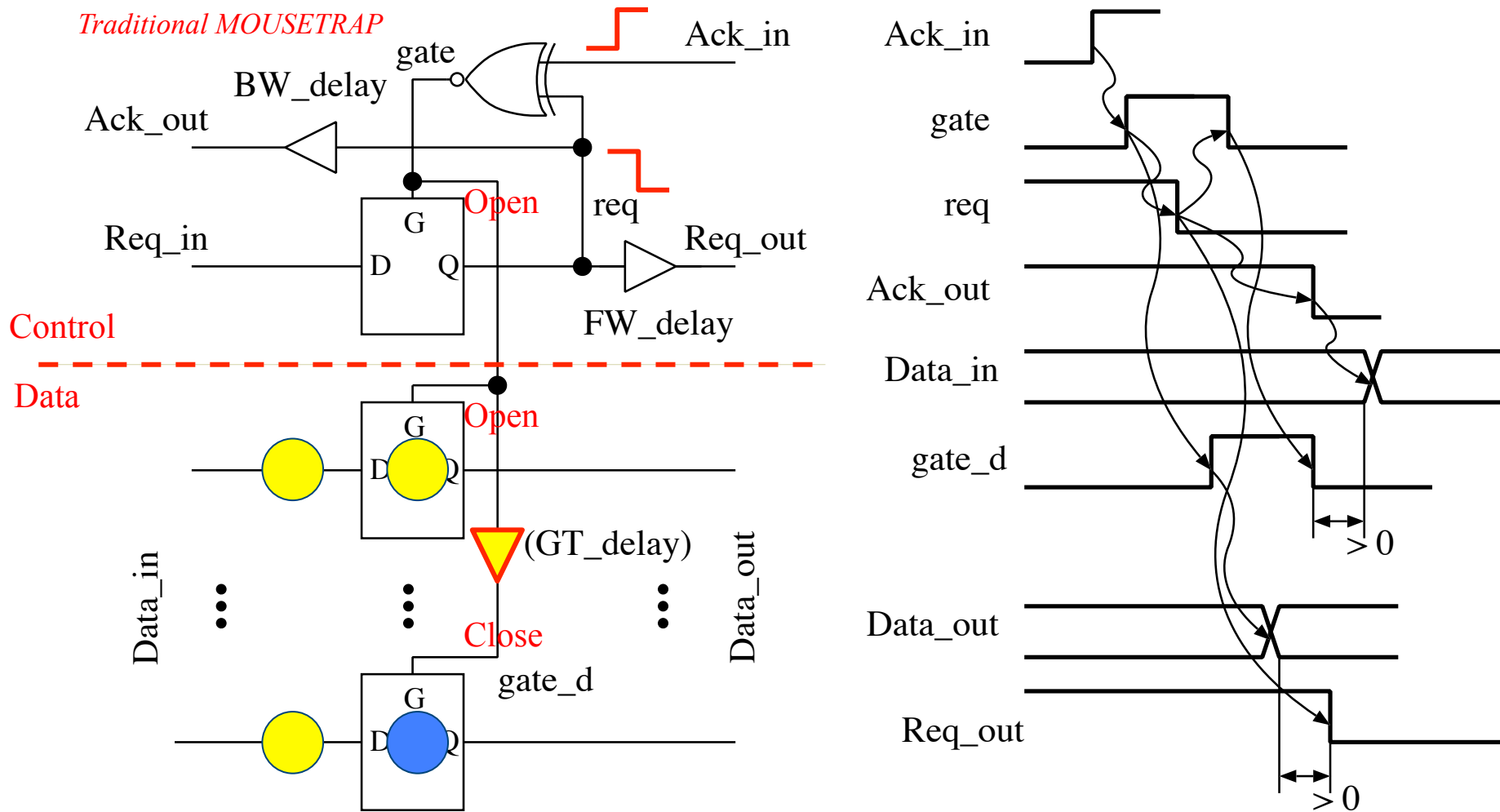
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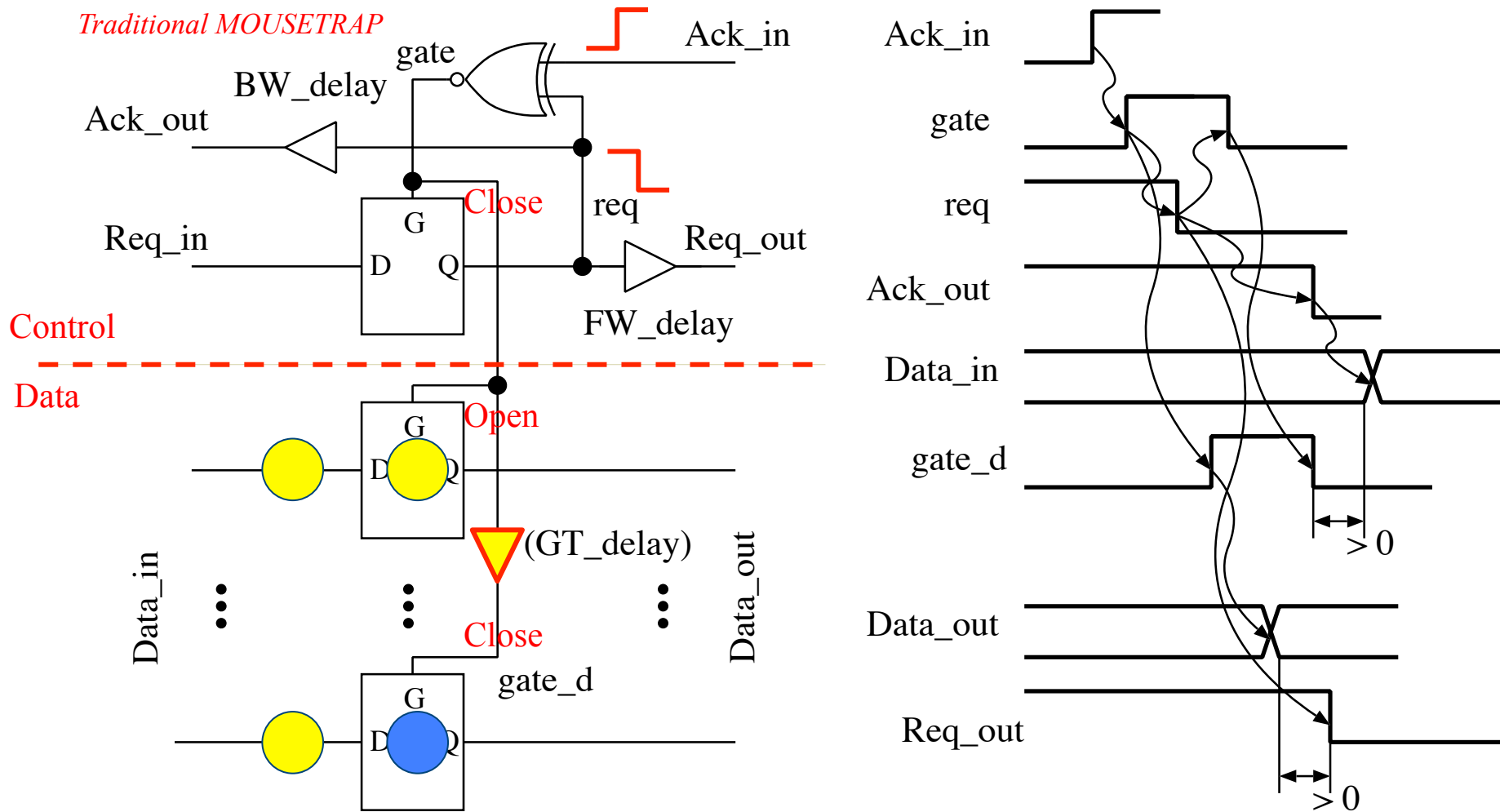
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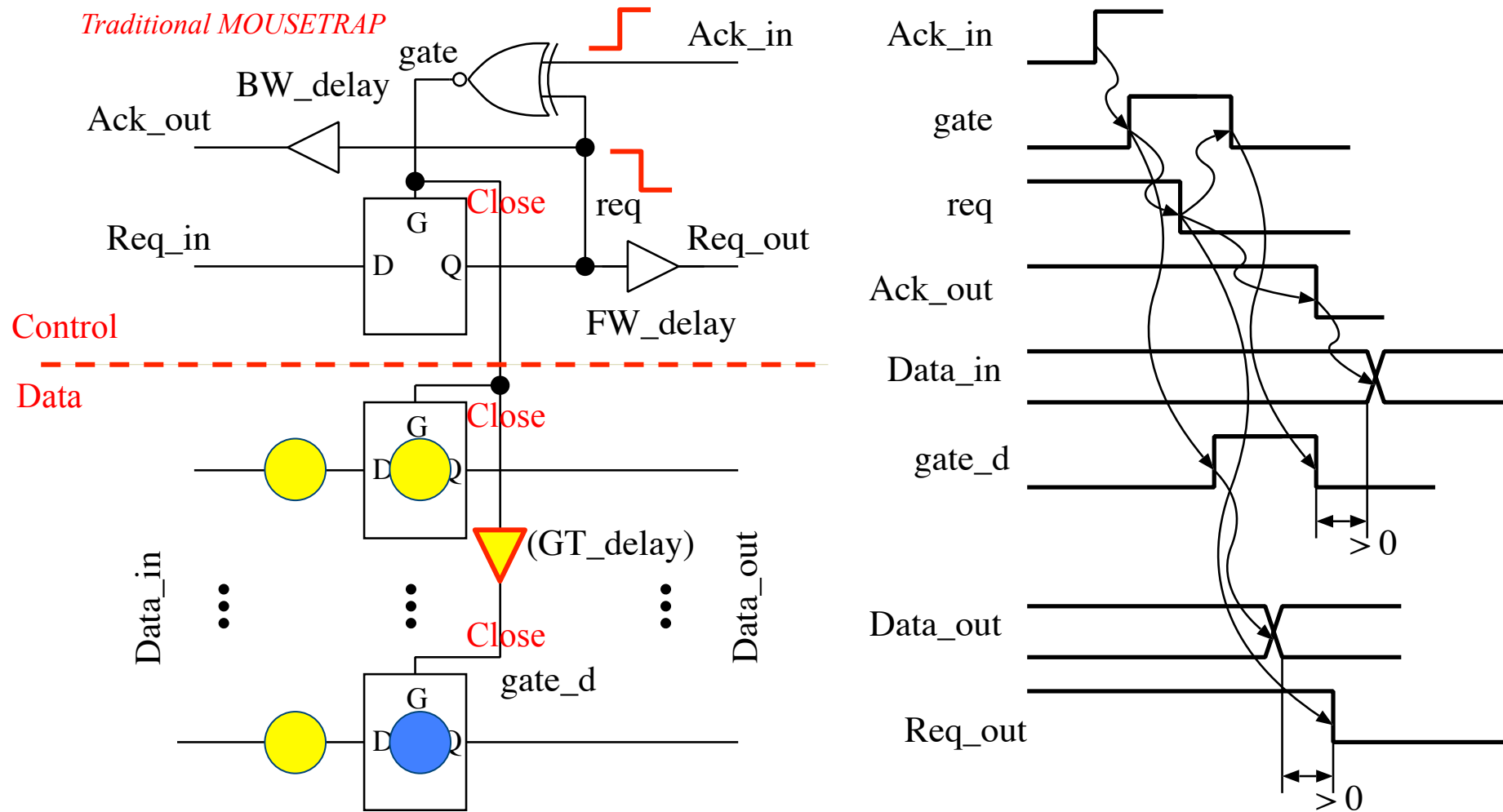
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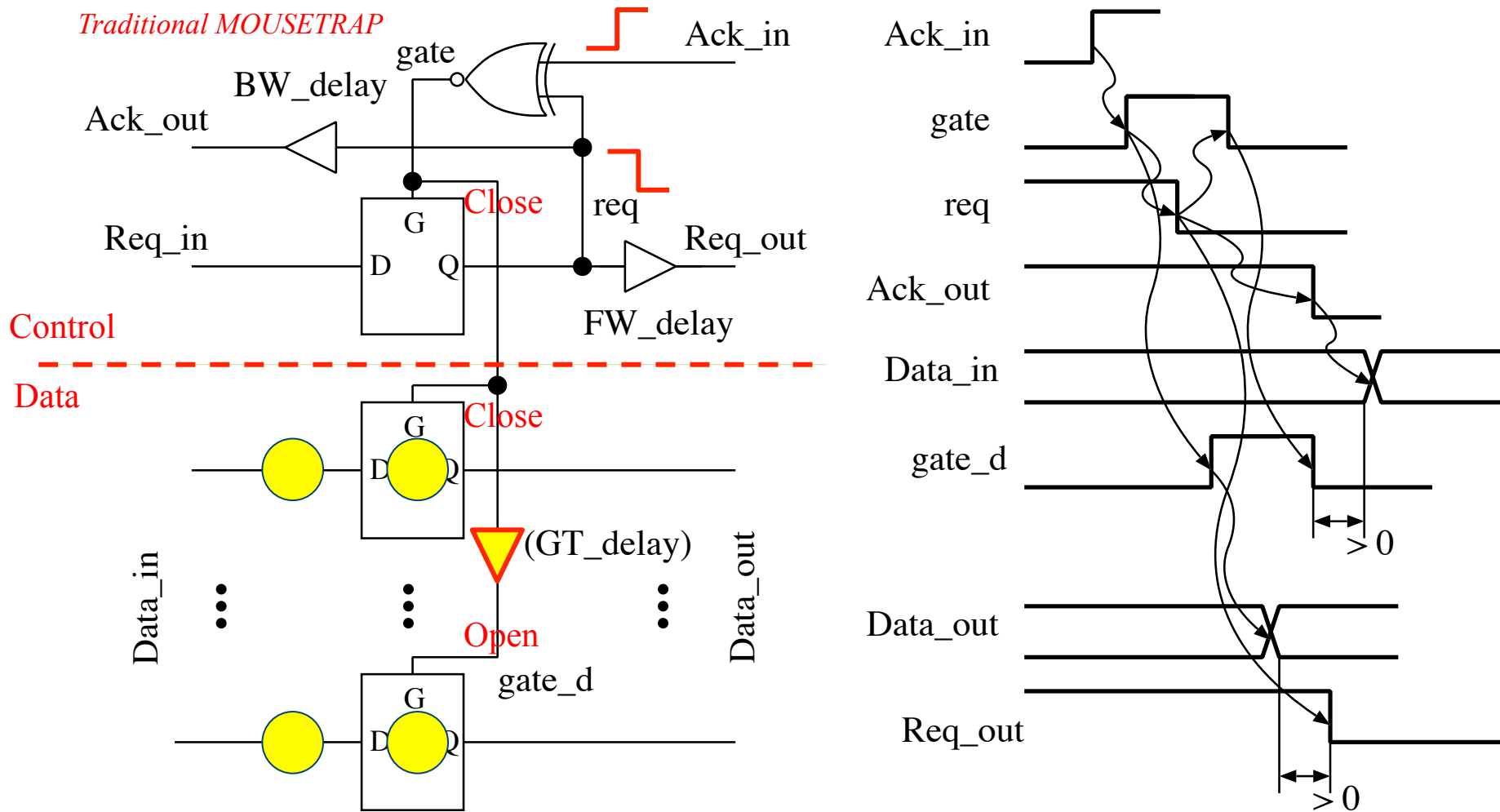
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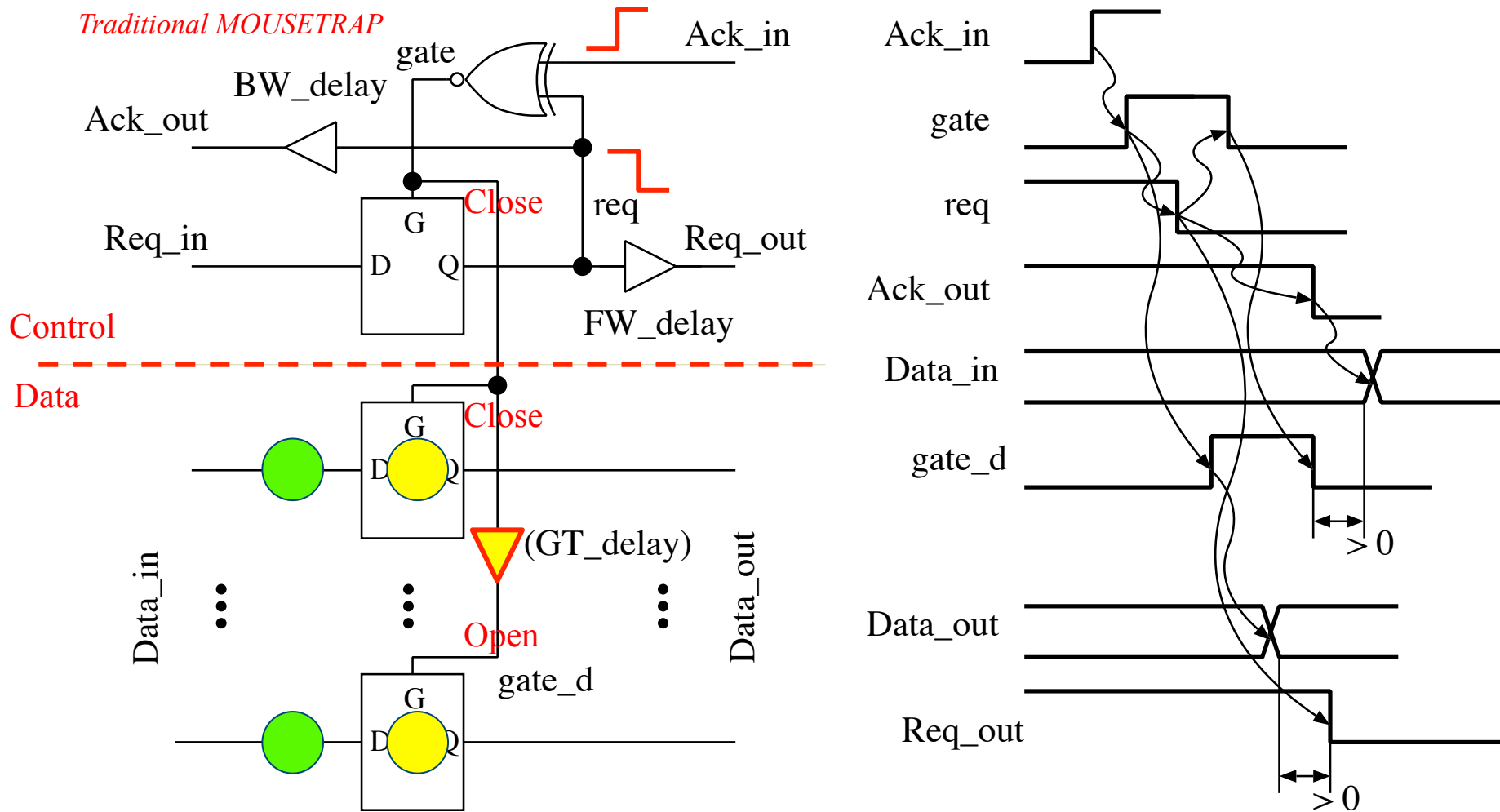
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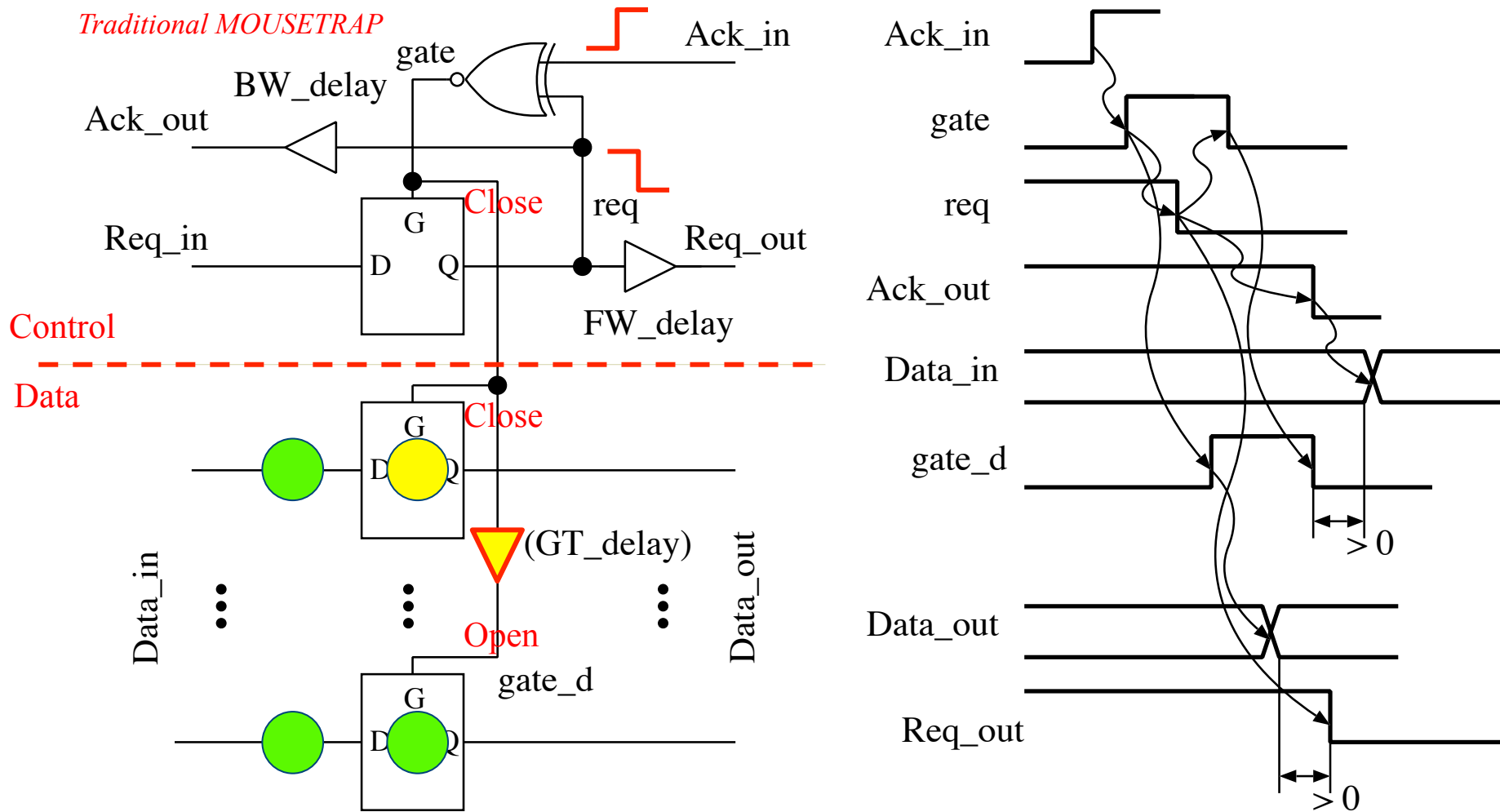
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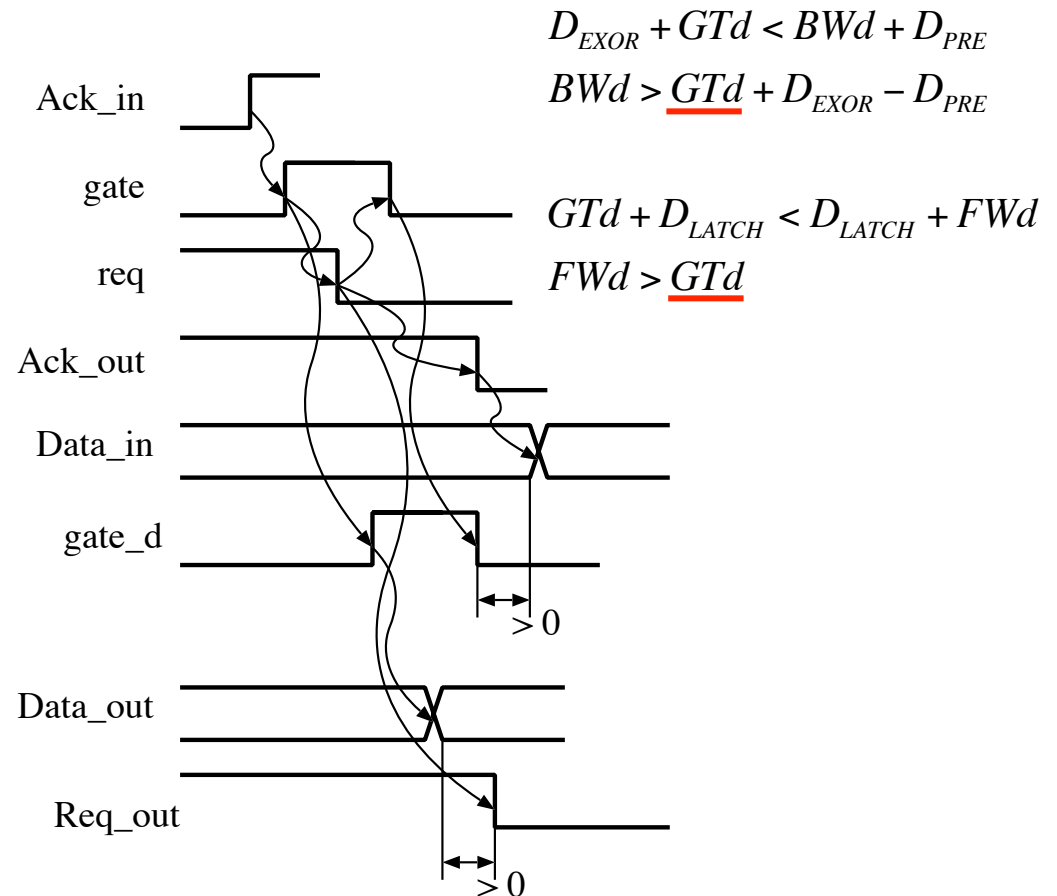
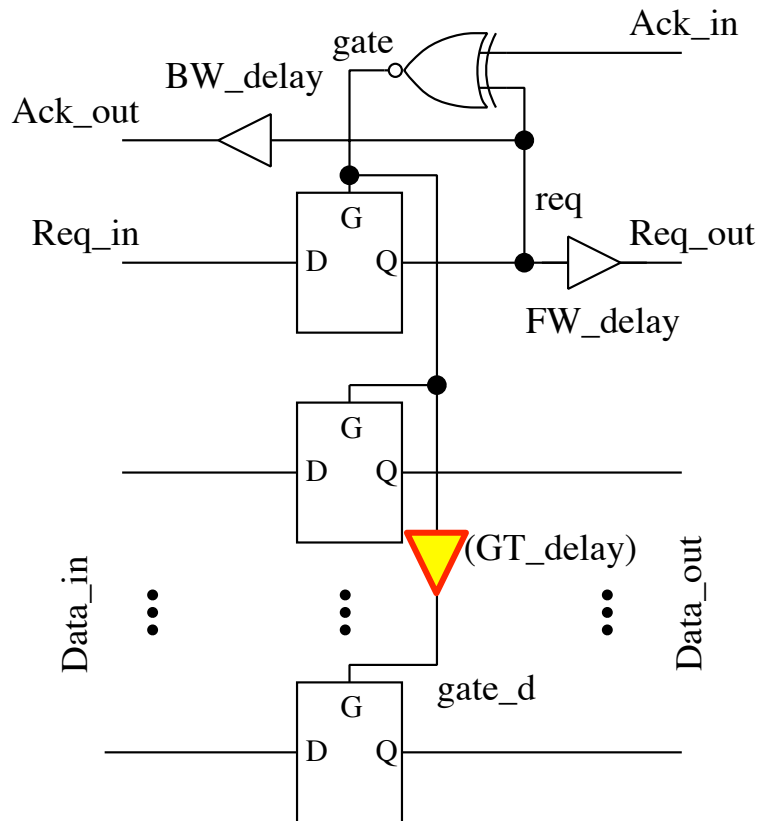
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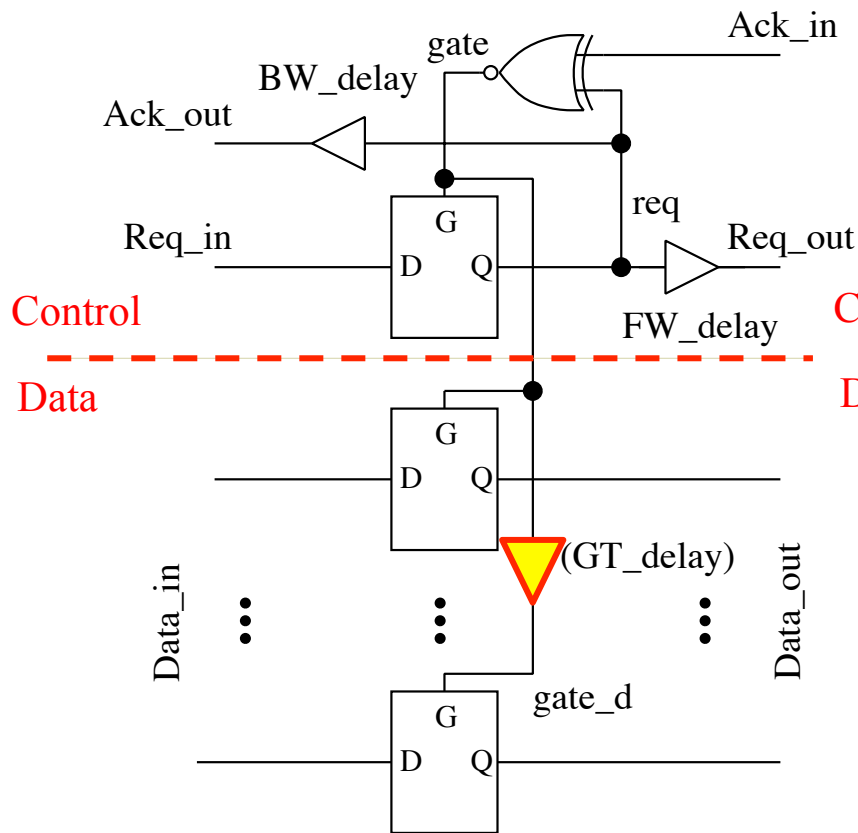


Delay issue in MOUSETRAP

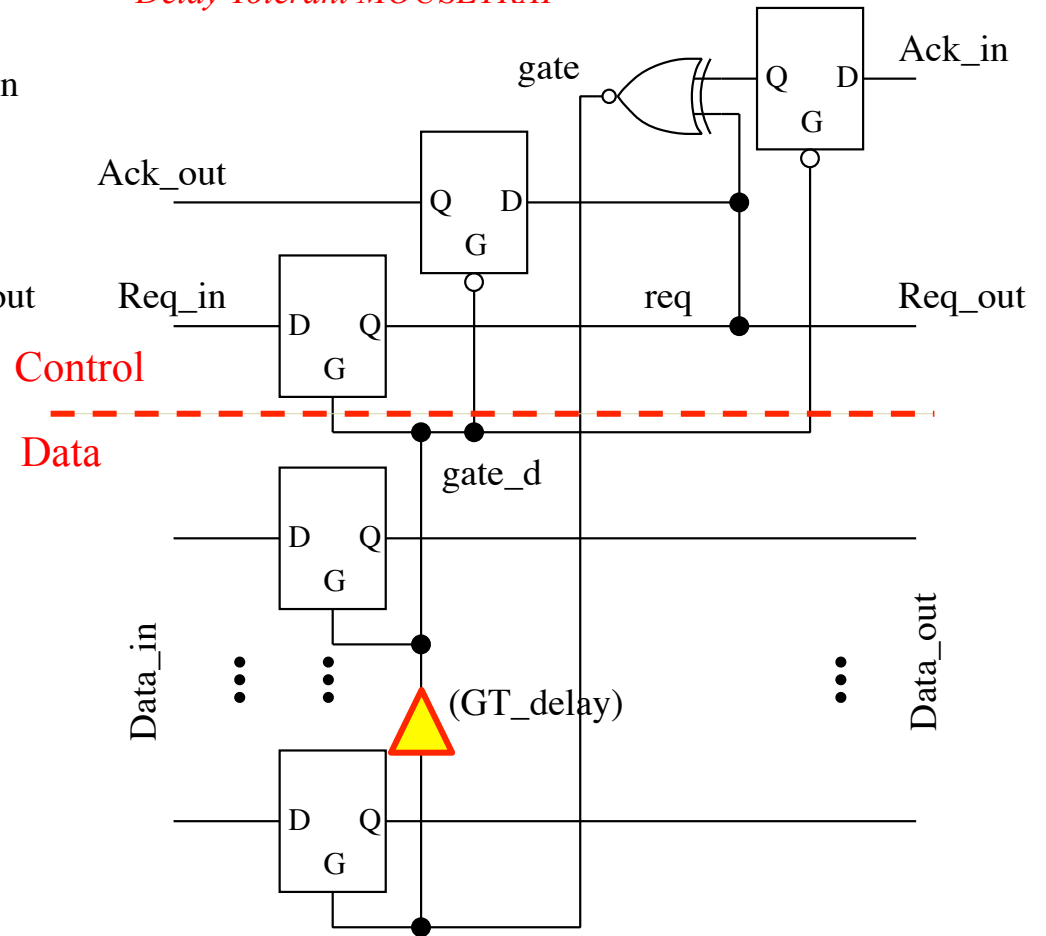


Delay Tolerant MOUSETRAP

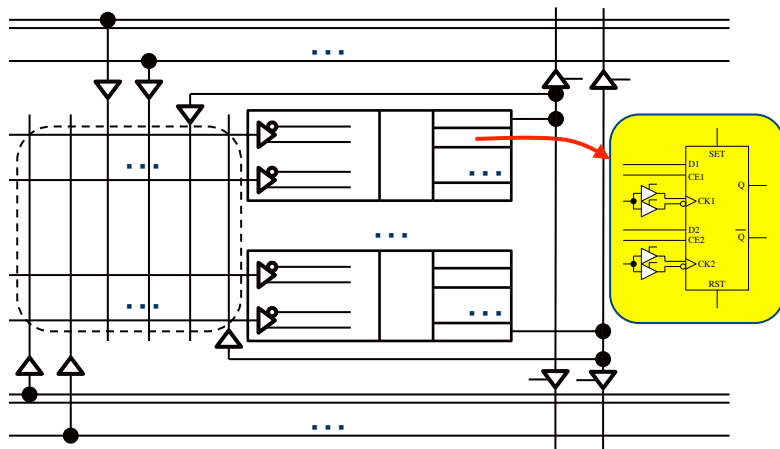
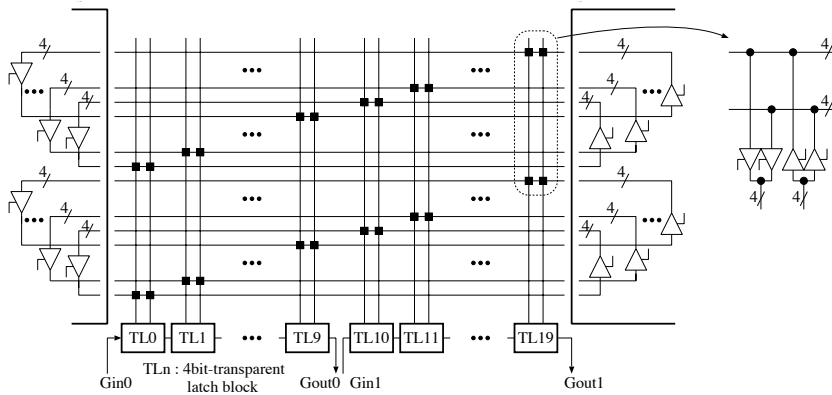
Traditional MOUSETRAP



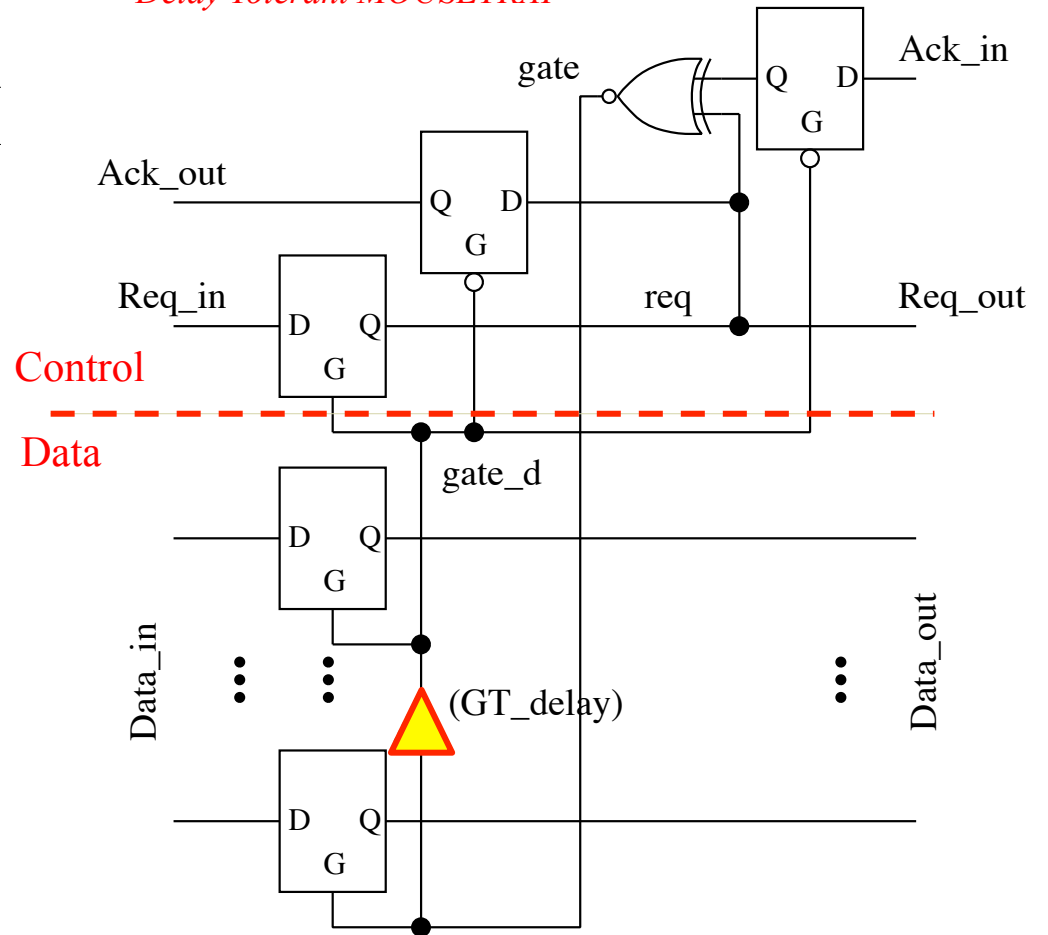
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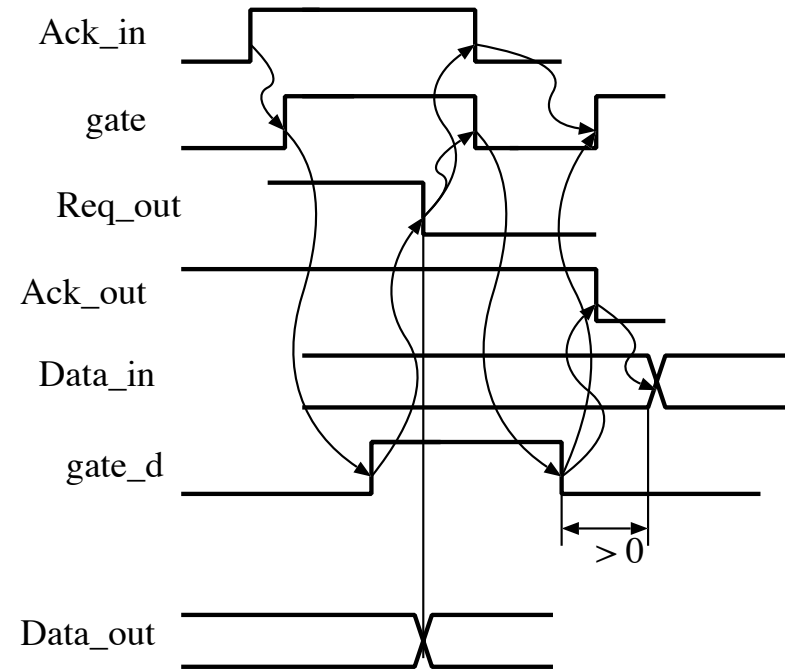
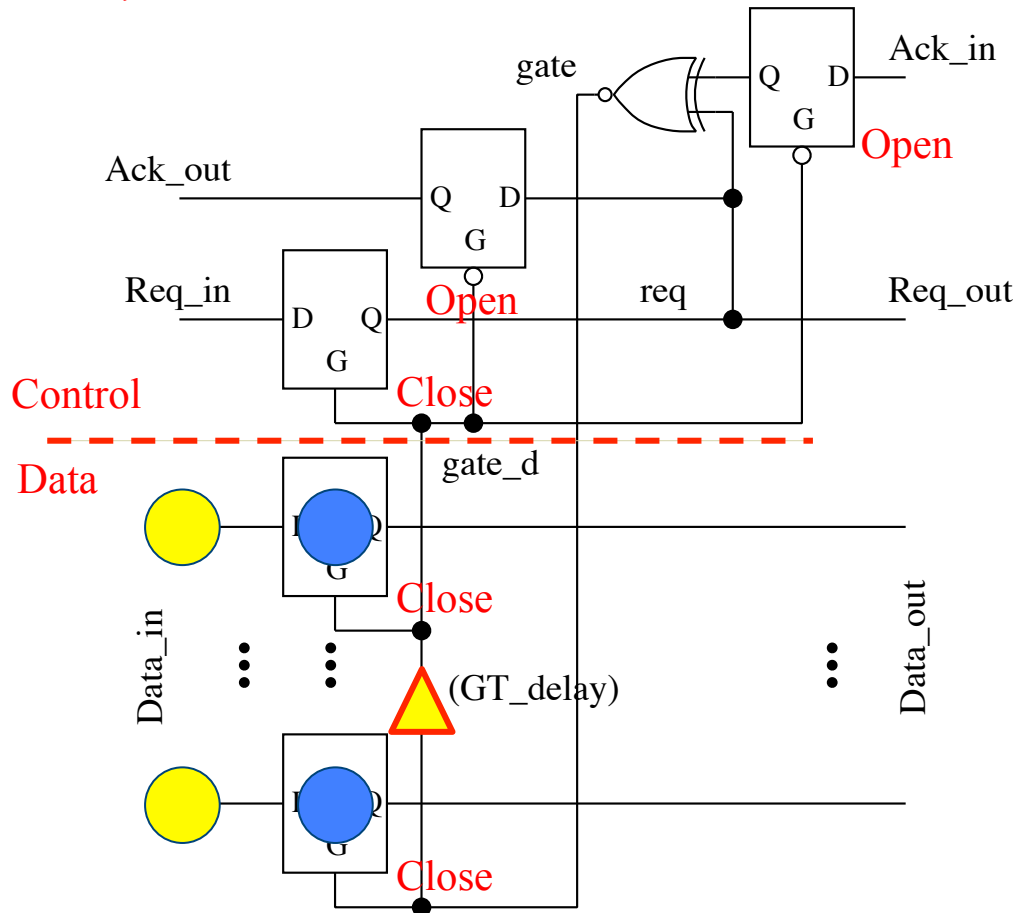


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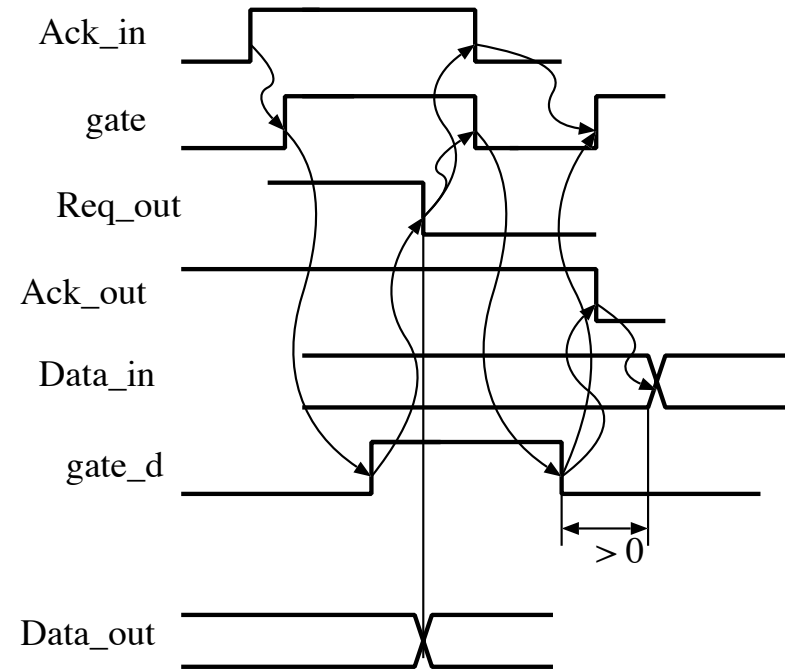
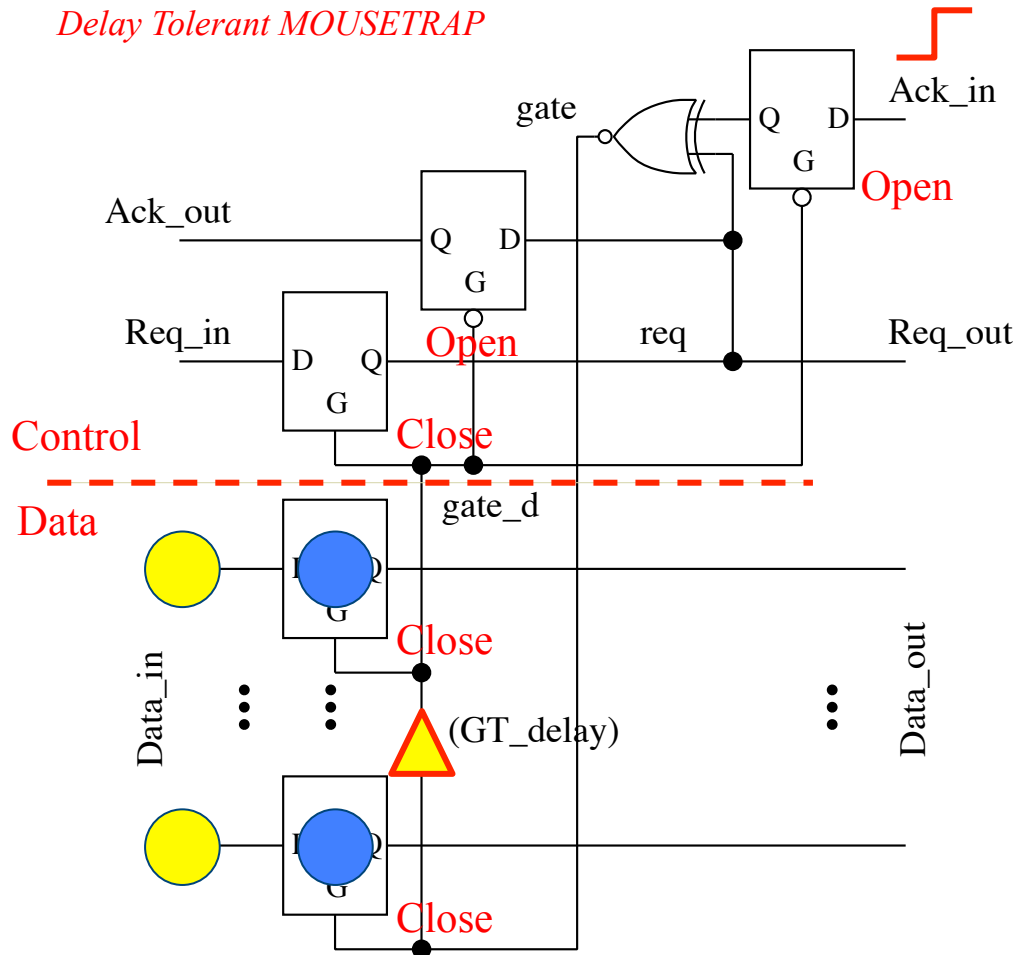
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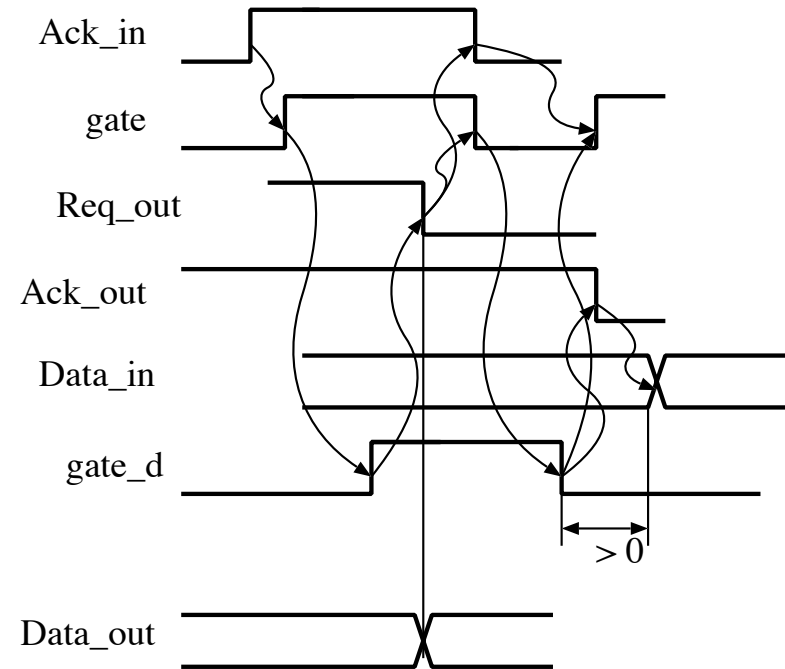
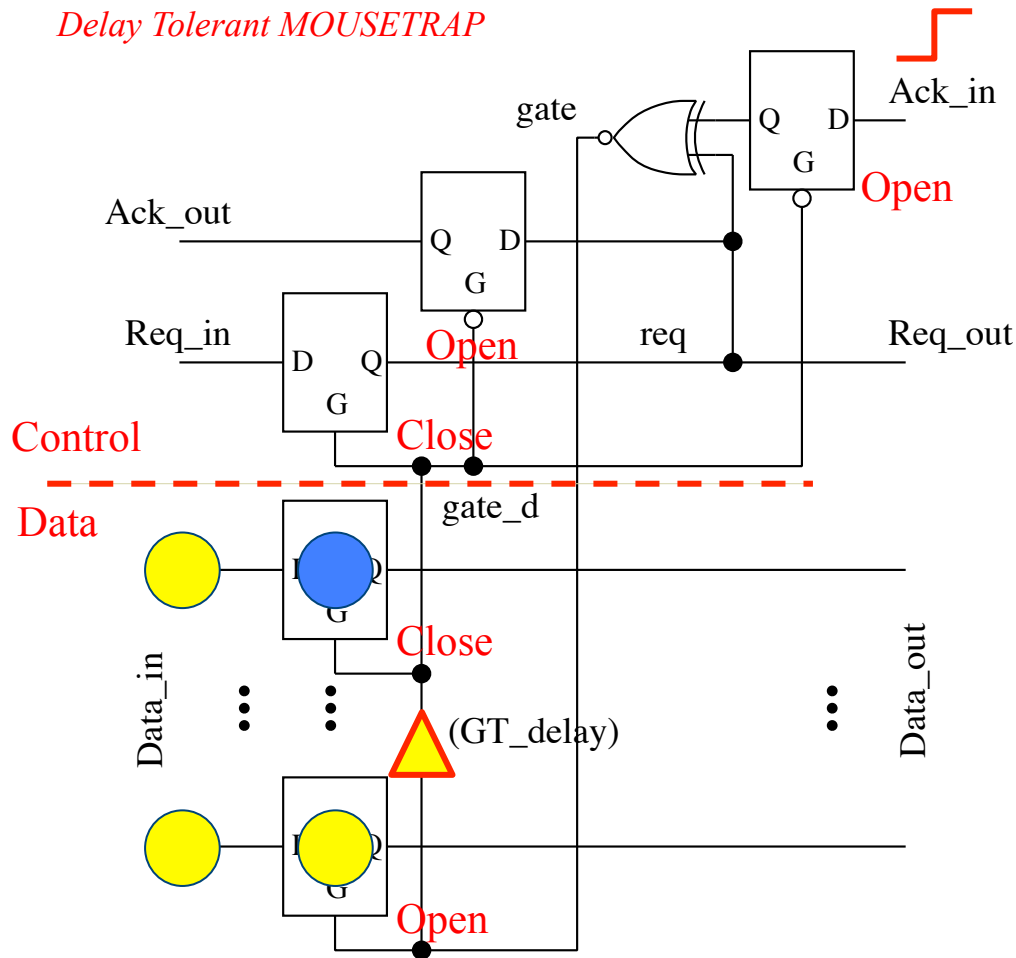
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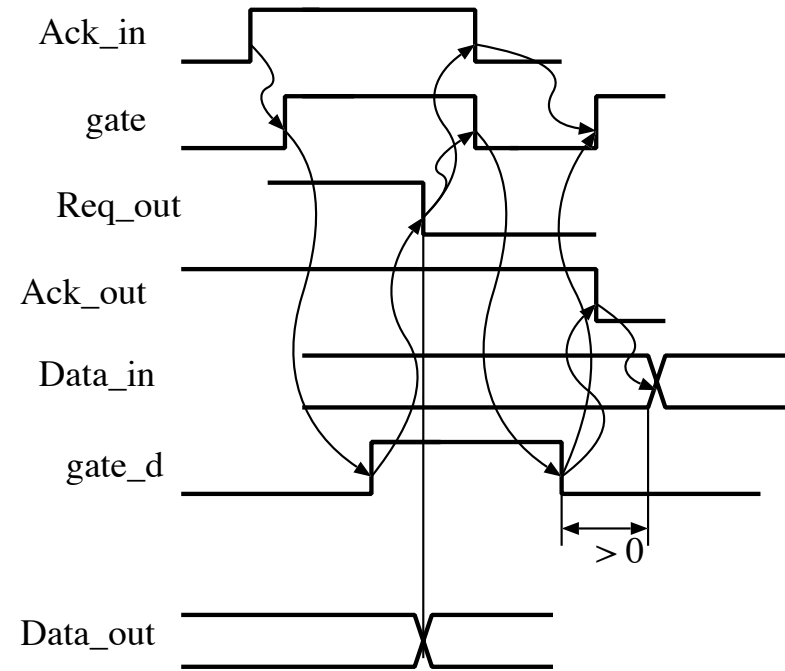
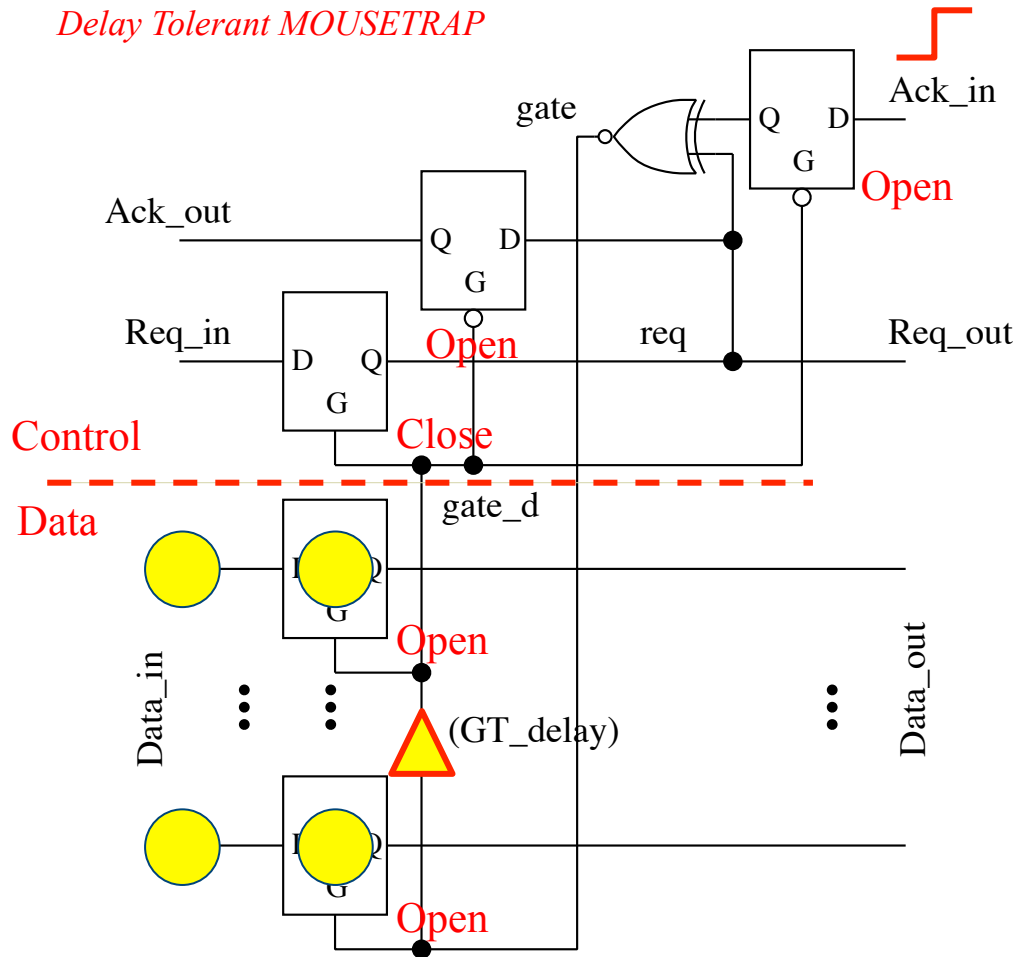
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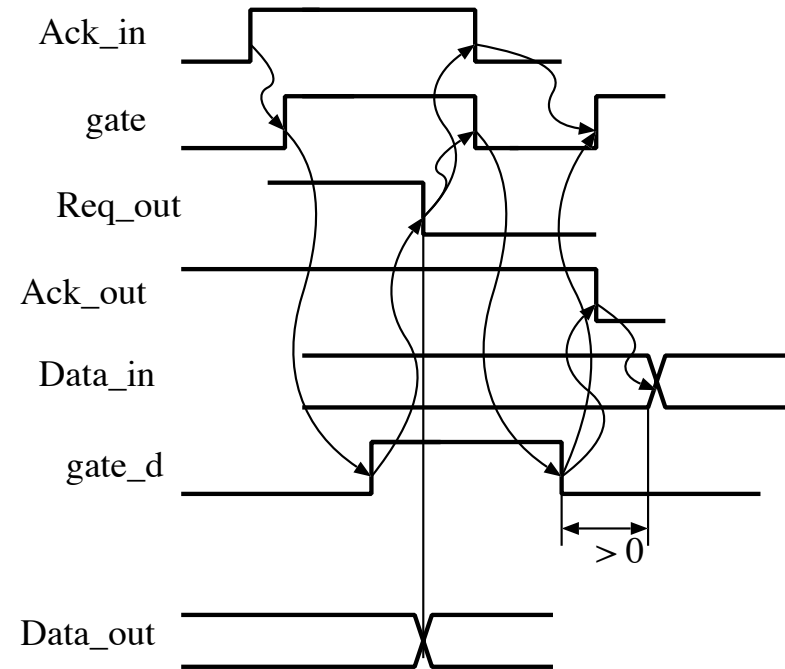
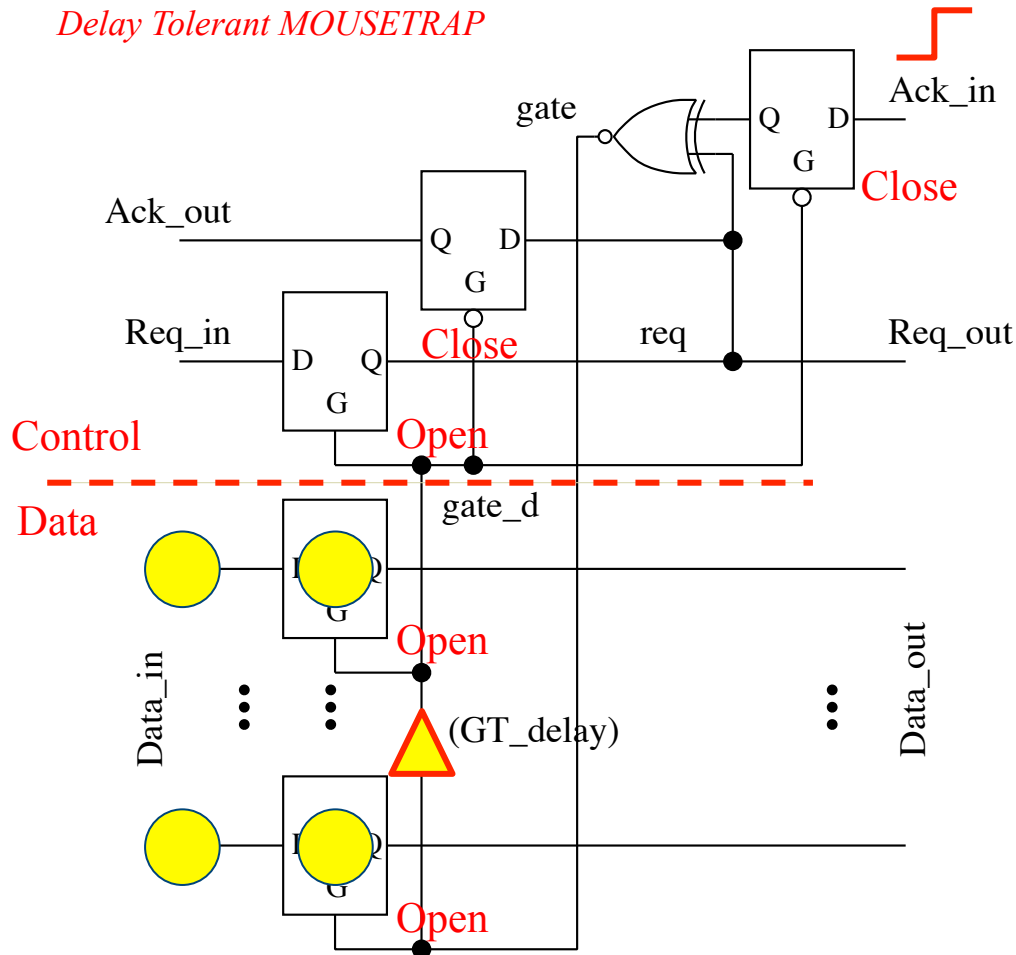
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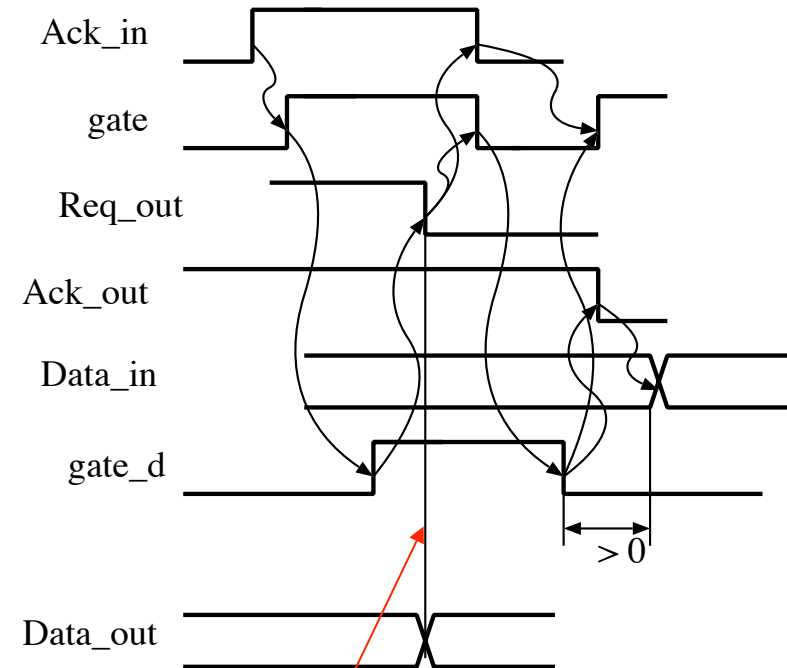
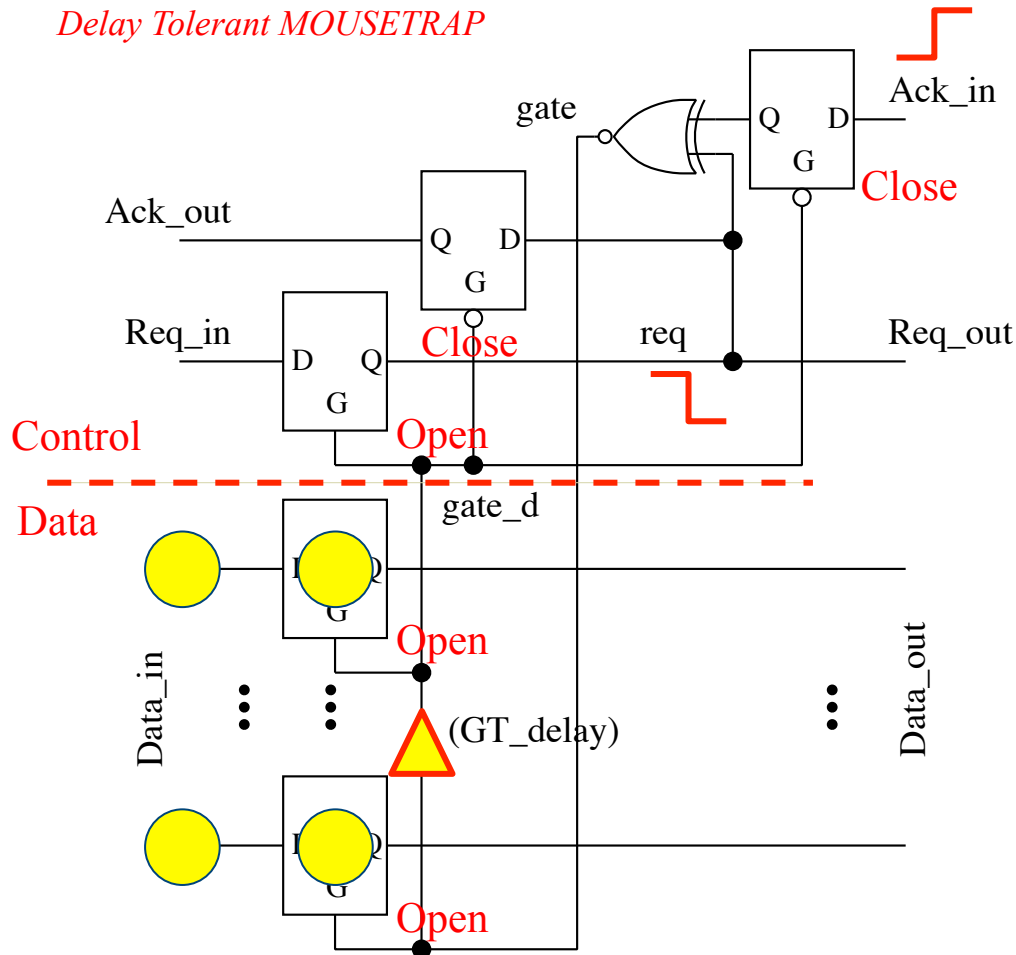
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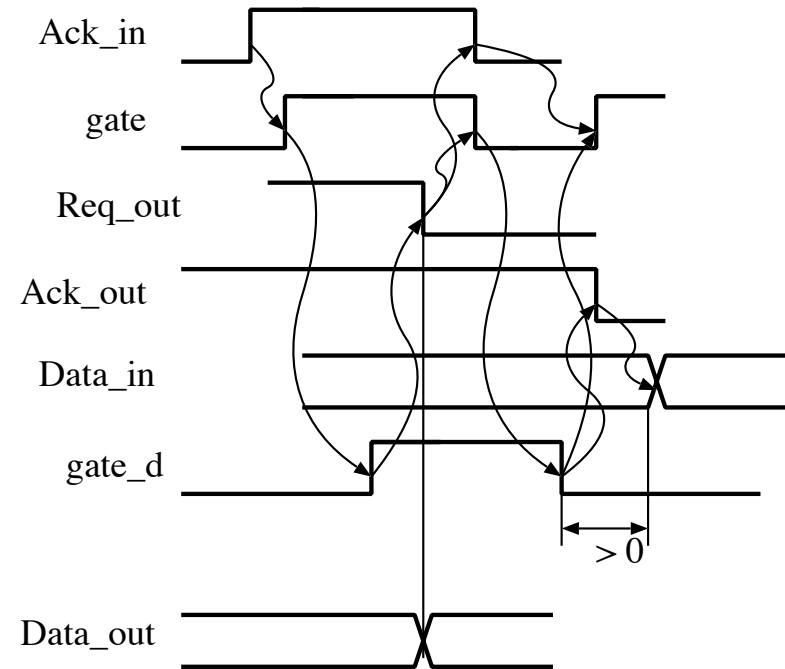
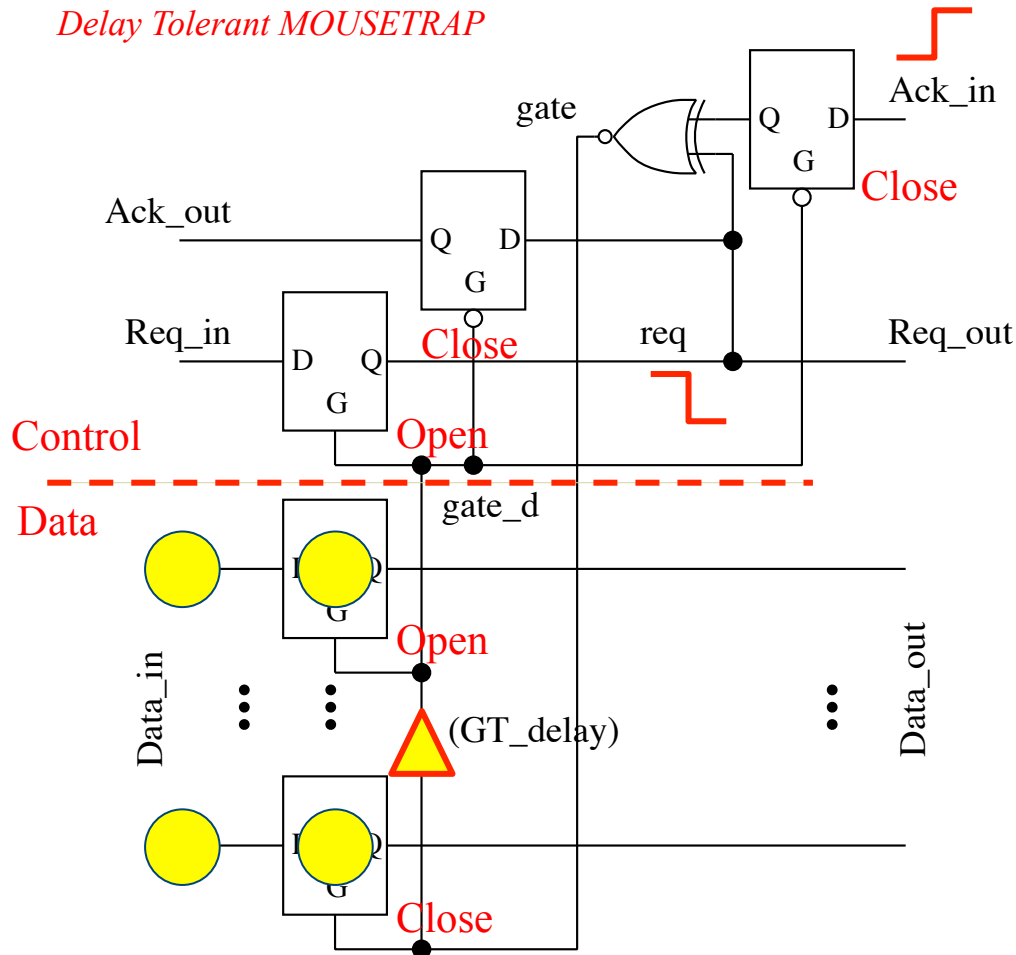
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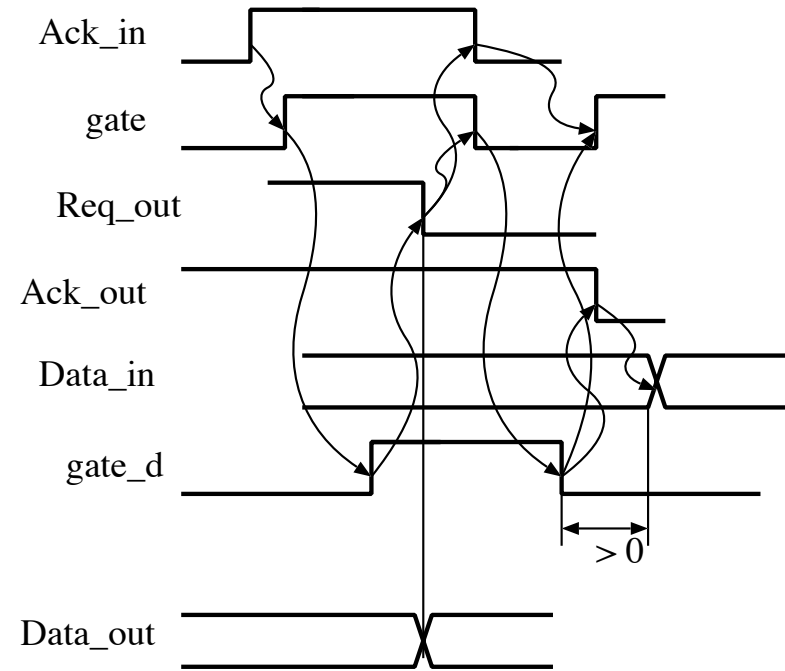
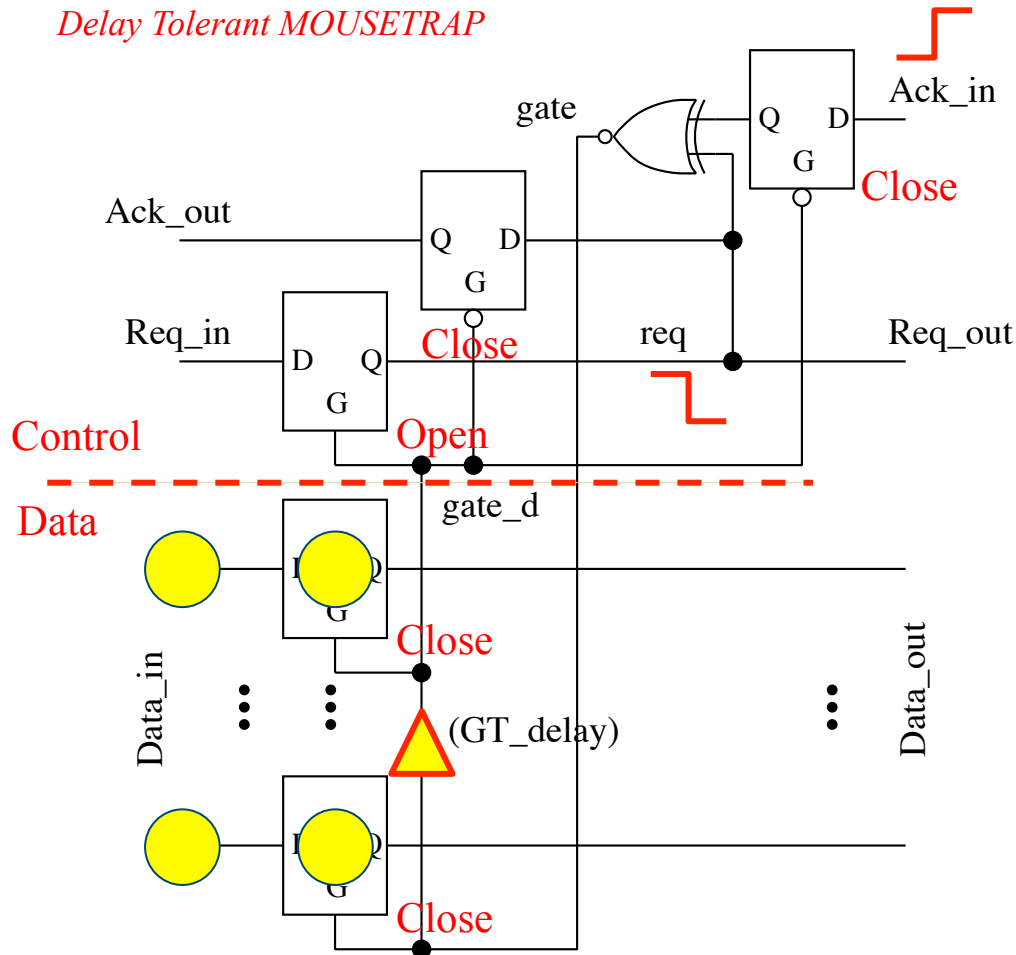
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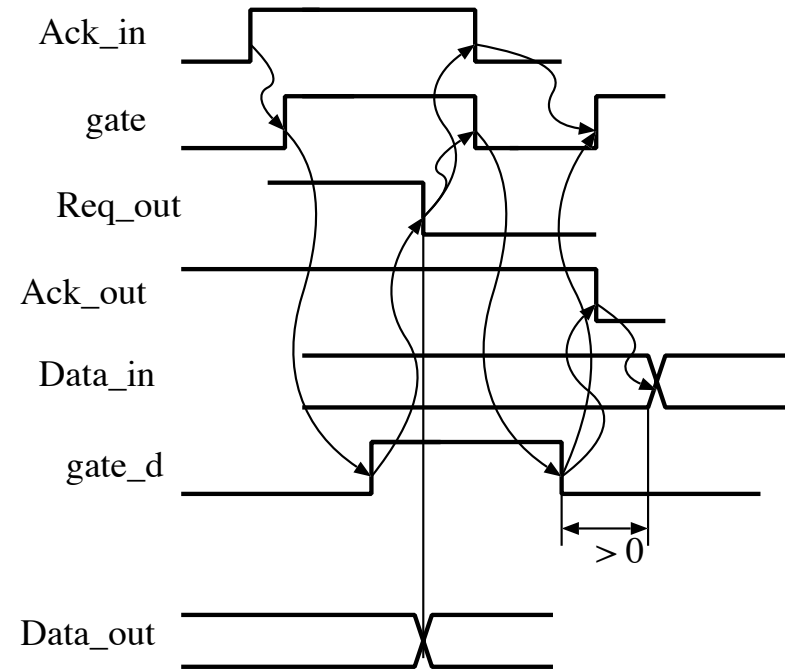
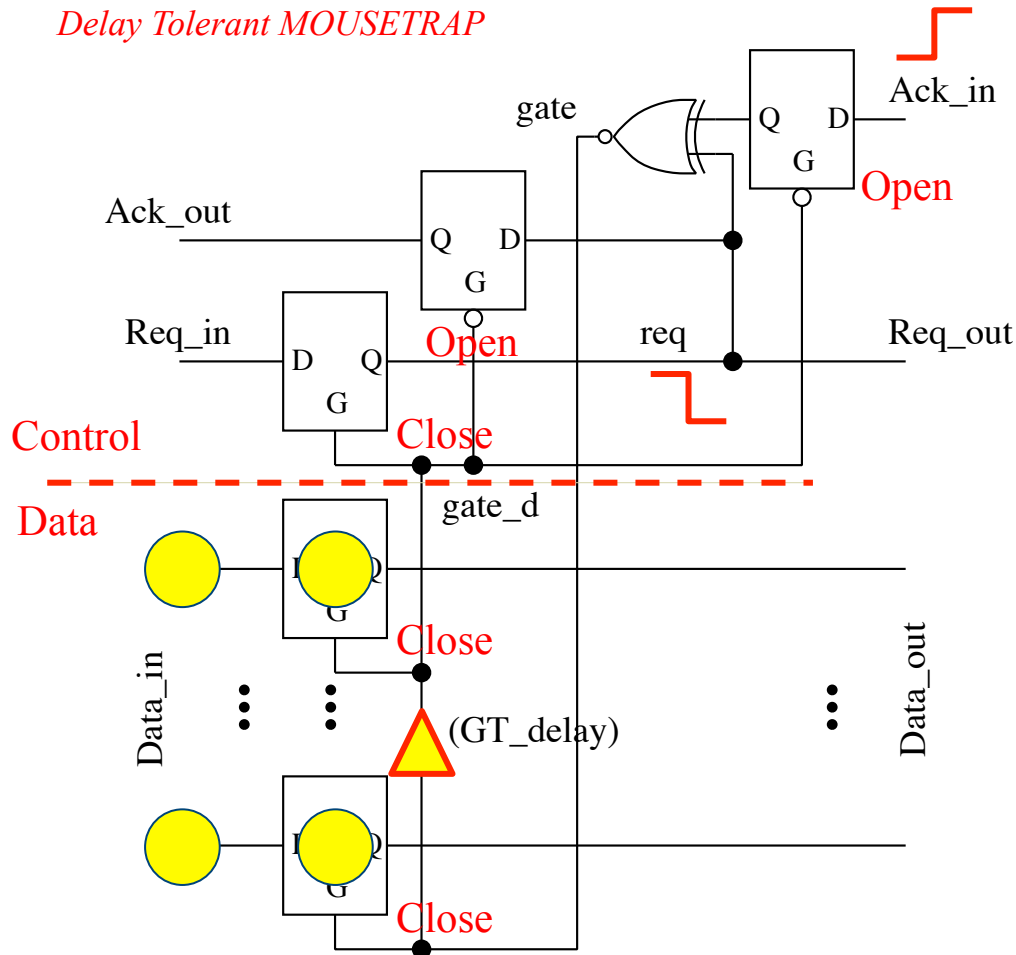
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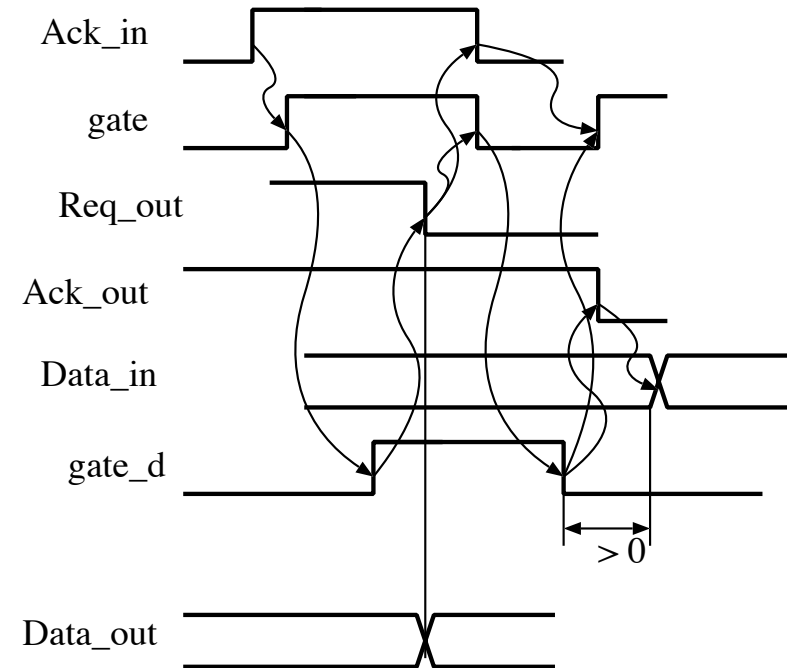
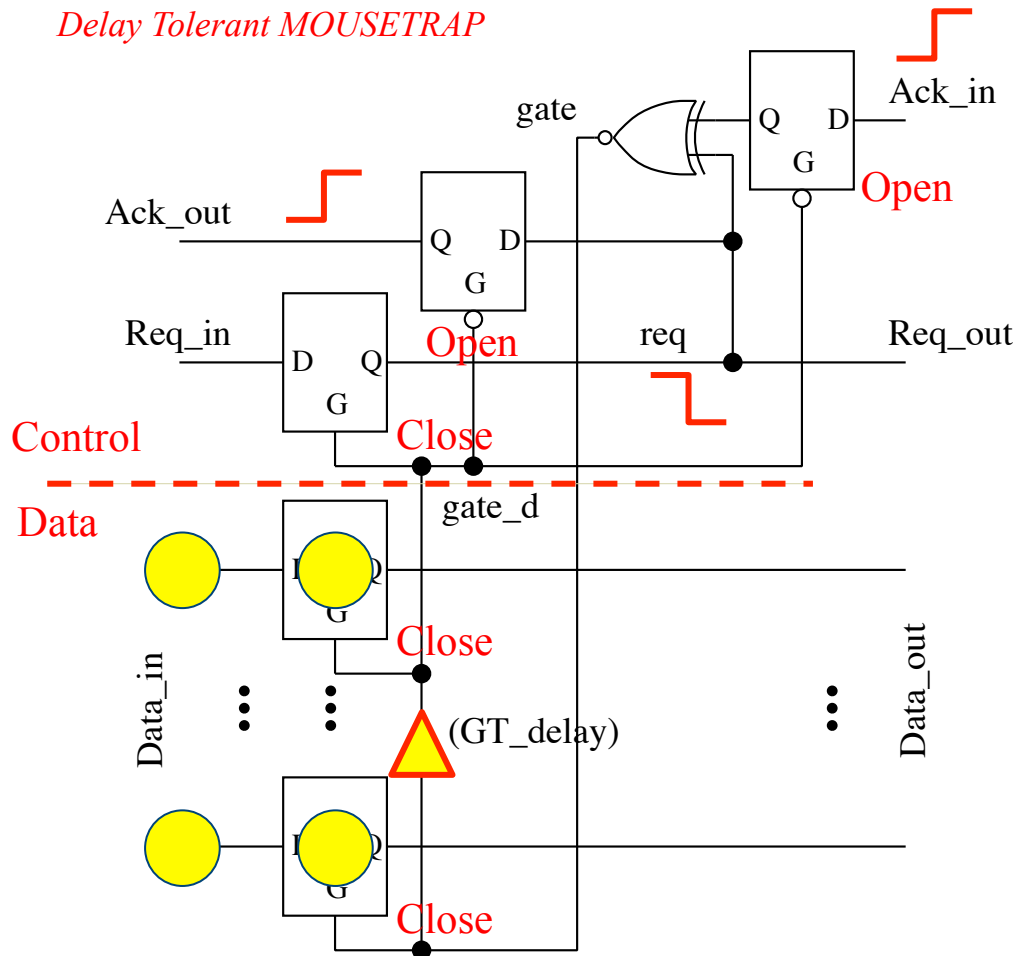
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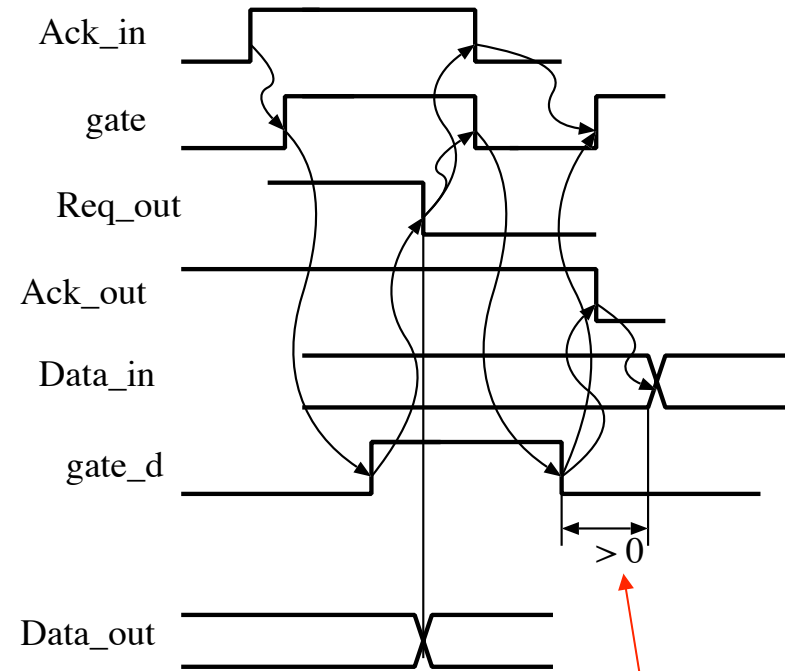
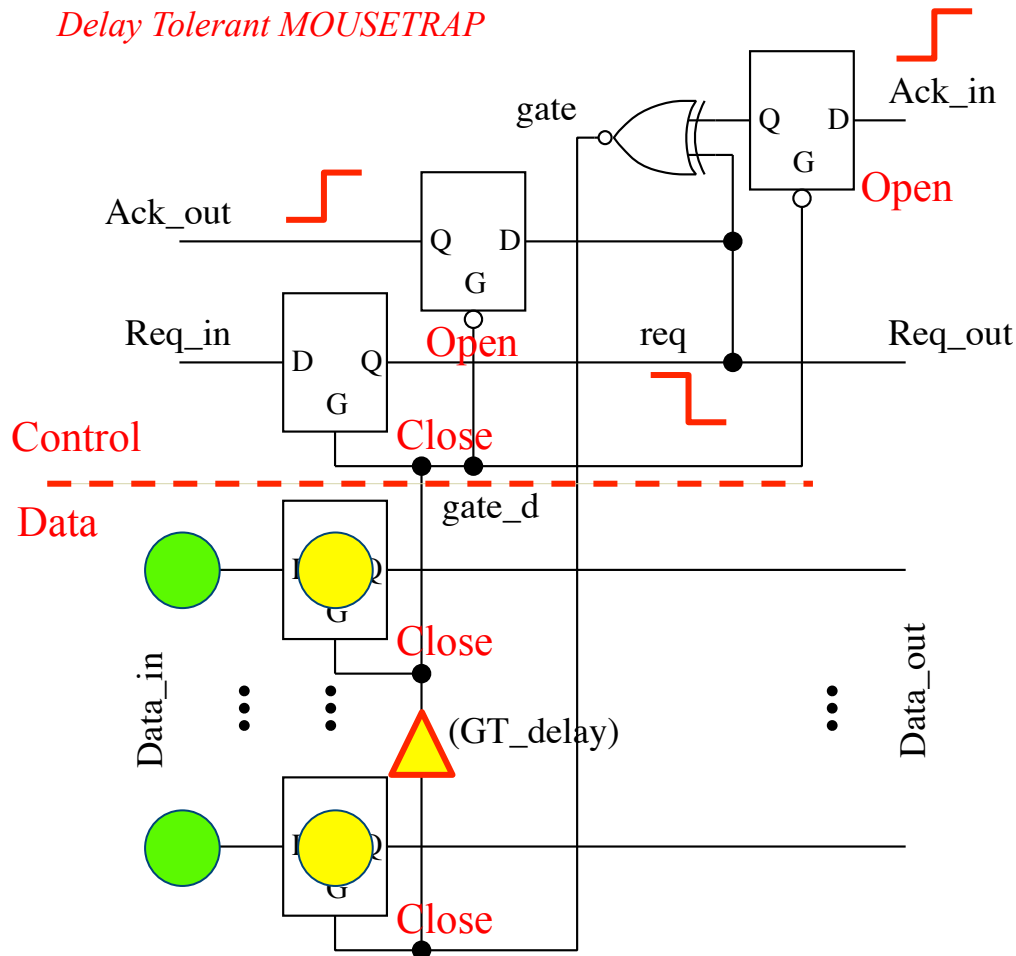
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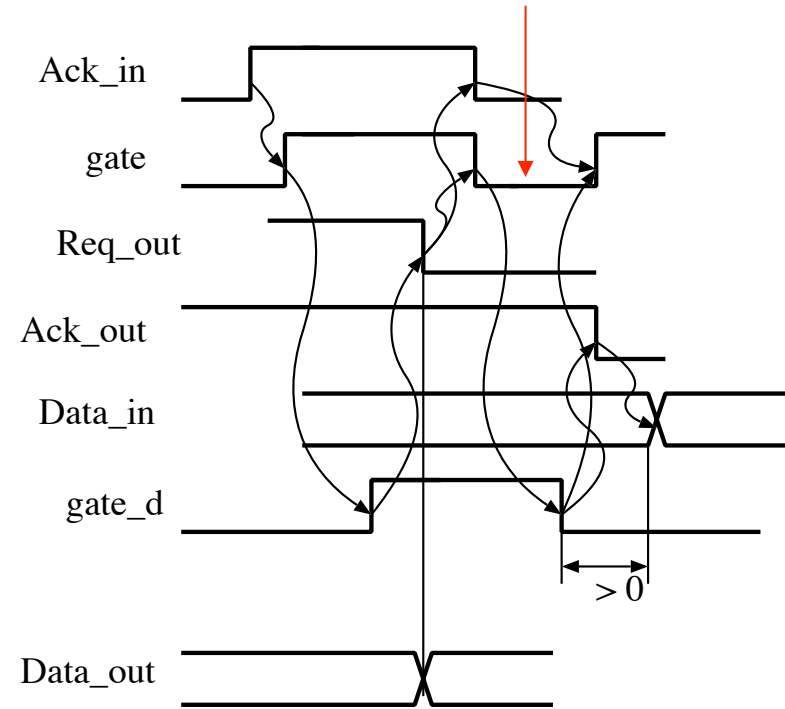
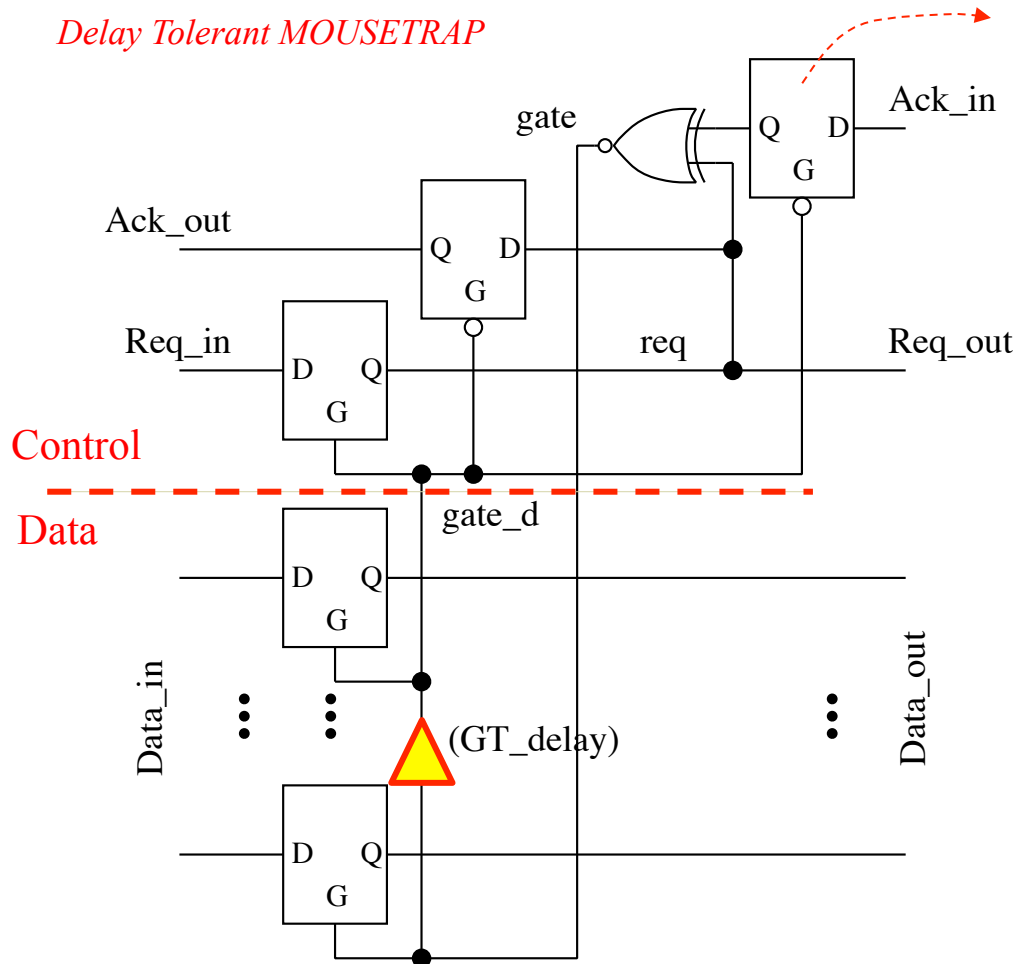


guaranteed by causality

Delay Tolerant MOUSETRAP

Delay Tolerant MOUSETRAP

used for avoiding too narrow negative pulse here



Current and Future work

- ◆ Interface to Sync. FPGAs
 - Pausible clock mechanism, ...
- ◆ Evaluation of performance, overhead, ...
- ◆ Estimation
 - Amount of control circuits
 - Amount of configuration memories
- ◆ ...
- ◆ CAD for reconfiguration

Thank You!