Hunting Asynchronous CDC Violations in the Wild

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CDC is the #2 Verification Problem

Flaws Contributing to Respins

Trends in Types of Flaws Resulting in Respins


* Multiple answers possible
Why CDC is a Big Problem: 10 or More Clock Domains are Common

Multiple Asynchronous Clock Domain Trends


H Foster, WRG Functional Verification Study, November 2014

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Even FPGA Users Are Suffering

Flaws Contributing to FPGA Rework

Trends in Types of Flaws Resulting in FPGA Rework

* Multiple answers possible


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The Scope of SoC Designs

- **Typical**
  - 100M gates total
  - 10 distinct IP blocks
  - 5-10 independent clock domains
  - 3-5 reset domains
  - 3-5 power domains (UPF)

- **Largest**
  - Over 1 billion gates
  - Over 100 distinct IPs
  - Over 150 independent clock domains
  - Over 10 reset domains
  - Over 10 power domains & voltage domains (UPF)
Types of Asynchronous Crossings

- **Clock domain crossing (CDC) paths**
  - Crossings between registers on asynchronous clock domains

- **Reset domain crossing (RDC) paths**
  - Crossings between registers on asynchronous reset domains

- **Voltage domain crossing (VDC) paths**
  - Crossings between registers on different voltage scaling domains
Common CDC Challenges

- **Design-related**
  - There are more than just asynchronous clocks
    - Mesosynchronous, Plesiosynchronous, Ratio-synchronous clocks
  - Impact of place-n-route on physical proximity
  - Power logic
  - Synthesis

- **Methodology**
  - Hierarchical vs. flat
  - Gate level CDC analysis
  - RTL to Silicon

- **User Errors**
  - Miscommunication: designer did not know there was a CDC path
  - Incorrect structure: designer made a mistake on the sync
  - Integration problem: 3rd party IP instantiated incorrectly
  - Misunderstanding / incorrect assumptions: violation incorrectly waived
  - Constraint setup errors: incorrect setup leads to incorrect results
Focus On: Hierarchical CDC

Why do Hierarchical CDC analysis?
- Capacity limitation
- Runtime
- Methodology
- Productivity

Non-technical challenges
- Blocks are implemented by different IP teams in different business units, geographies, or even different companies
- Handling encrypted IPs
- Data transfer from block to integration team (RTL vs. CDC model)

Productivity
- IP blocks developed and verified in parallel
- The SoC integration team often does not want to verify the blocks
- Block constraints may be extracted from top-level constraints
Hierarchical CDC Analysis Flow

**Top-down flow**

1. Top-level setups
2. Propagate top-level setups
3. Top-level CDC

**Bottom-up flow**

1. Block-level setups
2. Result

ASYNC 2015 - Questa CDC
Gate-Level CDC – RTL CDC is Inadequate

- **Synthesis may introduce CDC errors**
  - Glitchy logic
  - Retiming
  - Logic duplication

- **Checks required for DFT & Power logic**
  - UPF+RTL describe power-aware design
  - Checks for Clock & Power gating logic
  - Checks for BIST/Scan chains

- **Place-and-route**
  - Clocks that are synchronous still have skew due to propagation delay
    - Registers can be far apart in the chip – long delays
    - Clocks of different branches can have different propagation delays
    - Clocks may become asynchronous
  - MUX select signal may come in late
Technical Challenges

- Handle large SOCs, ASICs & FPGA-based designs
  - Today’s ASIC is next year’s IP

- Designs translate into huge directed graphs
  - Many million nodes, billion edges
  - Large sparse, with some strongly connected components

- Challenge: Solution should be close to linear
  - Standard graph algorithms apply: levelization, loop detection, min-cut, coloring, etc.
  - Large problem size requires careful implementation to be close to linear
The Future is Now: Asynchronous Crossing is more than CDC

Formal-based analysis is not just for CDC paths any more!

- **Power-Aware CDC**
  - Voltage domain crossing (VDC)
  - Power domains - includes isolation & retention cells

- **Reset Domain Crossings**
  - Crossings between asynchronous resets

- **Simultaneous multi-domain analysis**
  - Interacting CDC, RDC, VDC crossings
Summary

- CDC remains a big, unavoidable problem for customers

- Successful CDC verification of the chip is more than just technology – sound methodology is required too

- Numerous innovations in CDC technology & methodology will be needed to stay ahead of ASIC & FPGA trends
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