DD1: A QDI, Radiation-Hard-by-Design, Near-Threshold $18\mu W$/MIPS Microcontroller in 40nm Bulk CMOS

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Outline

- Overview
- Design and Test Results
- Reliability Analysis
- Conclusion
Designed, Built, Taped-Out, and Tested the World’s Lowest Power Radiation-Hardened MCU

- **200** times lower power than any other design built at the time
  - Similar speed
  - Similar radiation tolerance
- 40nm low-power bulk CMOS (TSMC 40LP)
- Atmel AVR reduced-core ISA compatible (e.g. ATtiny)
- QDI logic
- 95% yield on first silicon
- **Power and reliability**
**Tools, Architecture, and Layout**

- QDI: primarily PCHBs
- CHPSIM: CHP $\rightarrow$ structural Verilog
- Magic: custom 8-track standard cells
- Magic: full-custom memories & regfile
- 2KB IMEM, 256B DMEM, 16 I/Os
- 32x8b registers
- Supply range: 550mV to 1.1V
- 550mV: 18uW at 1 MIPS & 800nW at idle
Why Radiation Hard?

- Error rates increase as technology scales
- Error rates increase with altitude (aircraft & satellites)
- 14nm CMOS: 1 error every four days in 100Mbit SRAM (sea level)
- 14nm CMOS: 1 error every hour in 100Mbit SRAM (10km)

1 Hubert, G. et al.: Integration, Jan. 2015.
Effects of Radiation on CMOS Devices

- **SEU (single event upset)**
  - Problem: bit-flips in memory and logic
  - Mitigation: DD for logic, DICE for memories, physical separation of cells

- **SEL (single event latchup)**
  - Problem: transient or permanent well-based latchup
  - Mitigation: near-threshold operation, well separation

- **TID (total ionizing dose)**
  - Problem: gradual shift in $V_t$ resulting in timing variation
  - Mitigation: body biasing, QDI robustness to delay variation
SEU Mitigation (Random Logic)

- QDI
  - Input persistence
  - Acknowledgment of errant change on output of operators $F_a$ and $F_b$ blocked by C-element fence
SEU Mitigation (Random Logic)

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  - Acknowledgment of errant change on output of operators $F_a$ and $F_b$ blocked by C-element *fence*
SEU Mitigation (Random Logic)

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SEU Mitigation (Memories)

DICE
SEL & TID Mitigation

- No latchup: reducing $V_{DD}$ to near or below the nominal device threshold voltage, $V_t$, disables the n-p-n-p positive feedback path\textsuperscript{1}
- Near-threshold operation
  - The minimum energy operating point occurs near $V_t$
  - Reduced reliability and robustness
- TID
  - increased timing variation
  - (adaptive) body biasing and distinct voltage domains: shift operation back towards the TT corner

\textsuperscript{1}Harris et al.: CMOS VLSI Design, 2010
DD1 Cobalt-60 Test Results (TID)

* Test Facility - Kirtland Air Force Base
Heavy Ion Test Results (SEU/SEL)

800mV Heavy Ion Cross Section
Weibull Fit: W=45, L0=.75, S=0.92, SAT=3.5e-6

* Test Facility - UC Berkeley 88-inch cyclotron
Measured Energy/Instruction vs Supply Voltage

* Test Facility - Caltech lab
Measured MIPS vs Supply Voltage

* Test Facility - Caltech lab
Exactly Why Does QDI Fail Subthreshold?

- Reducing power and increasing robustness are in direct competition
- Fabricating and testing a microprocessor/ASIC is not sufficient
  - At what supply voltage does it fail, and why?
  - How do we optimize, *i.e.* reduce power and increase robustness?
  - Will it work in a future process?
- Primary difficulty: **Parameter Variation** and **Noise**
Parameter Variation

- Unavoidable
- Global variation (inter die)
  - Chemical mechanical planarization
  - Mask alignment
  - Ion implantation and annealing
- Local variation (intra-die)
  - Line edge roughness
  - Metal/Poly granularity
  - Random dopant fluctuation (RDF) \(^a\)
    - Dominates
    - Uncorrelated
    - \(V_t\) is a normal RV

\(^a\) Drago et al.: IEEE TSM May, 2009
\(^b\) Bernstein et al.: IBM JRD July, 2006
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Noise

- Unavoidable
- Physical noise
- Switching noise
  - Crosstalk
    - Capacitive coupling
    - Inductive coupling
  - Charge sharing
  - Power supply noise
- Noise tends to be proportional to $V_{DD}$
- Noise can be modeled as a DC voltage source between nodes

(Coupling Noise (40nm))
Noise and Parameter Variation Problems

- Both noise and variation can cause circuit failures
- Timing failures
  - Relative path delays (isochronic fork)
- Functional failures
  - Memories fail to hold state
  - Gates switch erroneously or do no switch at all
- Need to analyze and quantify these failure rates
Near-Threshold Model

\[ I_{on} = I_1 k_0 e^{k_1 \frac{V_{DD} - V_t}{n \phi}} + k_2 \left( \frac{V_{DD} - V_t}{n \phi} \right)^2 \]

- Physically derived\(^a\)
- Transregional
- Valid for NFET and PFET
- Validated across four different process technologies
- \( k_0, k_1, \) and \( k_2 \) are process independent
- **New fundamental model**

\(^a\)Keller et al.: IEEE TVLSI, 2014
Near-Threshold Statistical Delay

\[ I_{on} = I_1 k_0 e^{k_1 \frac{V_{DD} - V_t}{n\phi_t} + k_2 \left( \frac{V_{DD} - V_t}{n\phi_t} \right)^2} \]

- \( t_{pd} \propto \frac{V_{DD}}{I_{on}} \)
- \( V_t \) normally distributed
- \( t_{pd} \) log-non-central \( \chi^2 \)
- \( t_d = t_{pd} L_{dp} \) log-normal

(Path Delay Distribution)
Asynchronous Circuit Timing Failures

- Variation significantly alters path delay near-threshold
- Timing violations in QDI – exactly why and how?
  - Adversary path timing assumption is necessary and sufficient for correct QDI circuit operation
  - Formal proof\(^1\)
- Statistical timing model used to estimate probability of QDI timing violations

\(^1\)Keller et al.: IEEE ASYNC, 2009
Parameter Variation Reduces Robustness

- Gates *interpret* voltages at their input
- Parameter variation makes a gate more susceptible to noise causing a *misinterpretation*
- $G_1$ more robust than $G_2$ iff $G_1$ can tolerate more noise than $G_2$
- Quantify robustness and treat as first-order metric

(VTC Parameter Variation)
Static Noise Margin

- DC sweep input of gate → VTC parameters
- A gate-pair: $G_x$ driving $G_y$
- $NM_H = V_{OH}(G_x) - V_{IH}(G_y)$
- $NM_L = V_{IL}(G_y) - V_{OL}(G_x)$
- $SNM = \min(NM_H, NM_L)$
- A SNM at or below zero implies failure
- Statistical notion of SNM
  - $V_{IL}$ and $V_{IH}$ vary with of $V_t$

(VTC Parameter Extraction)
The Robustness Metric

- The probability that any gate-pair in a system has a NM less than a target \( NM_T \) (e.g. 10% \( V_{DD} \))

- Consider \( (INV_x, INV_y) \), a cross-coupled inverter-pair

\[
P(FAIL) = P(FAIL(INV_x, NM_T) \cup FAIL(INV_y, NM_T))
= P(SNM(INV_x, INV_y) \leq NM_T \cup
  SNM(INV_y, INV_x) \leq NM_T)
\]

- A constructive and composable definition
  - 1-Pair of inverters \( \rightarrow \) N-Pairs of inverters \( \rightarrow \) Chains of inverters \( \rightarrow \) Chains of inverting gates \( \rightarrow \) Any set of inverting gates

- Push through statistics and method of computation\(^2\)

\(^2\)Keller et al.: CSTR, 2015
DD1 Timing Failures

- 20K isochronic forks
  - 100 length-five adversary paths
  - 19.9K length-seven adversary paths
- Statistical delay model
- Failure: probability that isochronic path delay greater than length-five or length-seven adversary path

![Probability Density Plot]

- $t_{di}$
- $t_{da}$

Near-Threshold Hurdles
1/3 (New MOSFET Model)
2/3 (Timing Assumptions)
3/3 (Quantifying Robustness)

DD1 Analysis
DD1 Robustness Failures

- 120K equivalent gate pairs
- (NAND3, NOR3) worst-case upper bound
- Timing failure more likely than NM failure
  - No ratioed logic (staticizers)
  - Maximum stack of 4 FETs
Conclusion

- Designed, built, tested, & analyzed a full-custom radiation-hard by design QDI microcontroller
- Optimized for near-threshold operation
- Developed new models and methods of analysis to understand failure in the subthreshold & near-threshold operating regimes
Thank You!