ASYNC 2015

Call for Papers

21st IEEE International Symposium on Asynchronous Circuits and Systems
4-6 May 2015, Silicon Valley, California, USA | www.asyncsymposium.org

Today a large number of VLSI chips and digital systems designs contain multiple, interacting timing domains. The resulting asynchrony is both an opportunity and a challenge for design, validation, and test. The International Symposium on Asynchronous Circuits and Systems (ASYNC) is the premier forum for researchers to present their latest findings in the area of asynchronous design.

Regular Papers

Authors are invited to submit papers on any aspect of asynchronous design topics ranging from design, synthesis, and test, to asynchronous applications in system-level integration and emerging computing technologies. Topics of interest include:

- Mixed-timed circuits, GALS systems, Network-on-Chip, and multi-chip interconnects
- Elastic and latency-tolerant synchronous design
- Asynchronous pipelines, architectures, CPUs, and memories
- Asynchronous ultra-low power systems, energy harvesting, and mixed-signal/analogue
- Asynchronous logic in power-constrained applications
- Asynchronous techniques for 3D integration
- Asynchrony in emerging technologies, including bio, neural, nano, and quantum computing
- CAD tools for asynchronous design, synthesis, analysis, and optimization
- Formal methods for verification and performance/power analysis
- Test, security, and fault tolerance
- Asynchronous variability-tolerant design and design for manufacturing
- Circuit designs, case studies, comparisons, and applications

Submissions must report original scientific work, in 6-8 pages IEEE double-column conference format, with author information concealed. Accepted papers will be published in the IEEE digital library IEEEXplore and symposium proceedings.

Industrial Papers

ASYNC 2015 will include a special industrial workshop with papers and tutorials from industry and research on the state-of-the-art application of asynchronous designs to both existing and emerging technologies. The topics are targeted at industry and include:

- Synchronizers and clock domain crossing techniques
- Techniques for combining asynchronous and clocked designs
- CAD tools to integrate asynchronous circuits with clocked designs
- Circuit designs, case studies, comparisons, and applications

We solicit 1-to-2-page submissions for the workshop, IEEE double-column conference format. These papers will go through a separate light-weight review process. Accepted papers will be published in the IEEE digital library IEEEXplore and symposium proceedings.

A 1-day registration will be offered for the day of this industrial workshop.

"Fresh Ideas" Workshop / Tools & Demos

ASYNC 2015 will accommodate a special workshop to present "fresh ideas" in asynchronous design, not yet ready for publication. We solicit 1-to-2-page submissions for the workshop, which will go through a separate light-weight review process. Accepted submissions will be assembled in a binder and handed out at the workshop. We also solicit tools and demos for presentation at the conference.

Important Dates

Abstract Registration deadline:	24 Nov 2014
Full paper submission deadline:	1 Dec 2014
Notification of acceptance:	13 Feb 2015
Workshop paper submission deadline:	27 Feb 2015
Publication-ready final version due:	6 Mar 2015

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