Call for Papers
19th IEEE International Symposium on Asynchronous Circuits and Systems
May 19-22, 2013

Santa Monica, California, USA

The International Symposium on Asynchronous Circuits and Systems (ASYNC) is the premier forum for researchers to present their latest findings in the area of asynchronous design. The symposium will be hosted by USC at the Double Tree Hotel in Santa Monica, southern California.

Authors are invited to submit full papers on any aspect of asynchronous design, ranging from the core topics of design, synthesis, and test, to asynchronous applications in system-level integration and emerging computing technologies. Topics of interest include, but are not limited to:

1. Mixed-timed circuits, GALS systems, Network-on-Chip, and multi-chip interconnects
2. Elastic and latency-tolerant synchronous design
3. Synchronization, clock domain crossing, arbitration, and metastability
4. Asynchronous pipelines, architectures, CPUs, and memories
5. Asynchronous ultra-low power systems, energy harvesting, and mixed-signal/analogue
6. Asynchrony in emerging technologies, including bio, neural, nano and quantum computing
7. CAD tools for asynchronous design, synthesis, analysis, and optimization
8. Formal methods for verification and performance/power analysis
9. Test, security, and fault tolerance
10. Asynchronous variability-tolerant design and design for manufacturing
11. Circuit designs, case studies, comparisons, and applications

SPECIAL TRACK: Industrial Aspects of Clock Domain Crossing and Synchronization.

We also solicit papers for the special track. Papers submitted for consideration to the special track will receive the same standard of peer review as regular papers. When evaluating a paper submitted to the special track, the Program Committee will give extra consideration to the contribution of the paper to the topic of the track.

The topic of the special track pertains to issues of clock domain crossing and synchronization in industrial applications, solutions applied by the industry, and solutions offered by EDA and IP core providers. All types of clock relationships are of interest.

In addition to papers submitted for review, we may also invite papers from industry.

PAPER FORMAT AND SUBMISSION: Papers must not exceed EIGHT (8) pages in IEEE double-column conference format (single-spaced, 10pt or larger font size). Submissions shorter than 8 pages are acceptable (especially for the industrial track). All papers will be evaluated based on the overall merit of their contributions to theory and/or practice, innovation, relevance, and presentation. New idea and new topic papers are strongly encouraged. Accepted papers will be published in the IEEE digital library and in the symposium proceedings.

> **Important:** ASYNC 2013 is running a blind review process. In preparing your manuscript, do not include any information which could reveal your identity, or that of your co-authors. The title section of your manuscript should not contain any author names, email addresses, or affiliation. If you do include any author information on the title page, your submission will be automatically rejected. In the body of your submission, you should eliminate all direct references to your own previous work. That is, avoid phrases such as "this contribution generalizes our results for XYZ." Also, do not disproportionately cite your own previous work. In other words, make your submission as anonymous as possible. We need your cooperation in our effort to maintain a fair blind review process, and to consider all submissions equally.

Symposium website: http://ee.usc.edu/async2013 or http://asyncsymposium.org

Submission website: https://www.softconf.com/d/async2013/

Important Dates

Abstract registration deadline	Dec 7, 2012
Full paper submission deadline	Dec 14, 2012
Notification of acceptance	Feb 22, 2013
Publication-ready final version due	Mar 15, 2013

Program Co-Chairs

Tomohiro Yoneda, National Institute of Informatics, Japan (yoneda@nii.ac.jp)
Ran Ginosar, Technion, Israel (ran@ee.technion.ac.il)