Cadence Virtuoso Tutorial

version 6.1

University of Southern California

Last Update: Oct, 2015

EE209 – Fall 2015

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System Setup

Basic setup

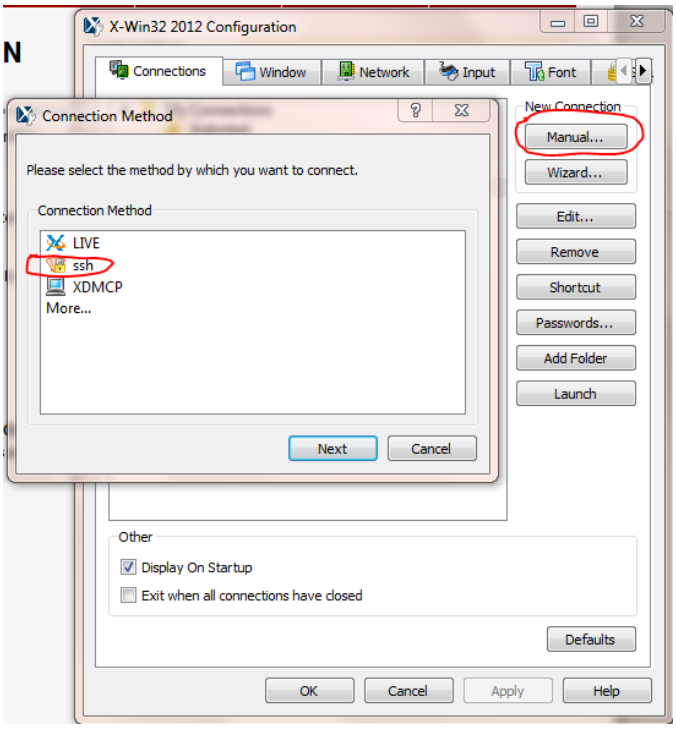
Cadence can only run on the unix machines at USC (e.g., viterbi-scf1). You will need to remote login (XTerm) to these machines to run the tools.

- If you're using Windows, download X-Win32 2012 (for remote login) and Filezilla (for file transfer) from http://software.usc.edu (usc account login required)
- If you're using MAC or Ubuntu, use terminal command "ssh -X" for remote login and "scp" or "sftp" for file transfer. If you're not familiar, please read this tutorial for more information: http://www.linuxtutorialblog.com/post/ssh-and-scp-howto-tips-tricks

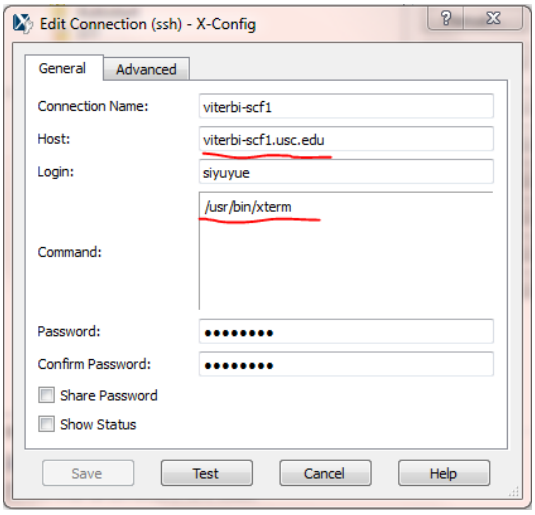
  If you have any license issues when you run X-Win32, you can either try to connect to USC Wireless Plus (how-to link: http://www.usc.edu/its/wireless/plus/) or use USC VPN (how-to link: http://www.usc.edu/its/vpn/anyconnect.html).

a) X-Win32 Connection Setup

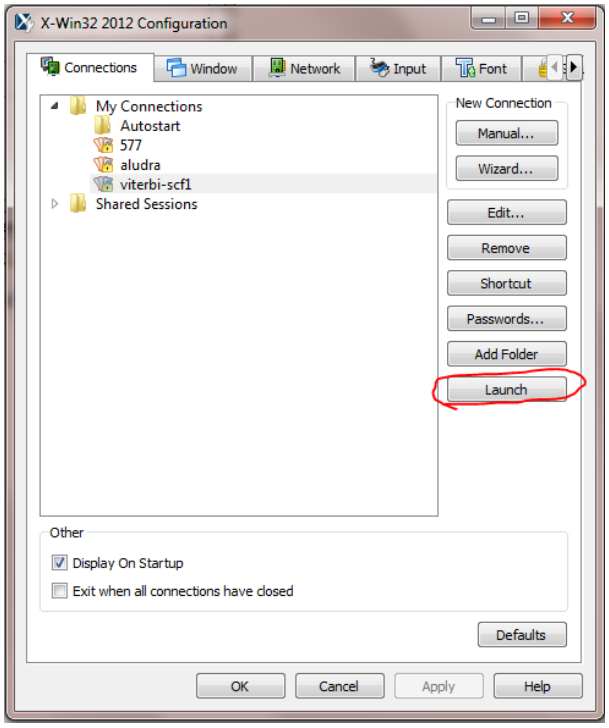
To remote login using X-Win32, select Manual and choose ssh:



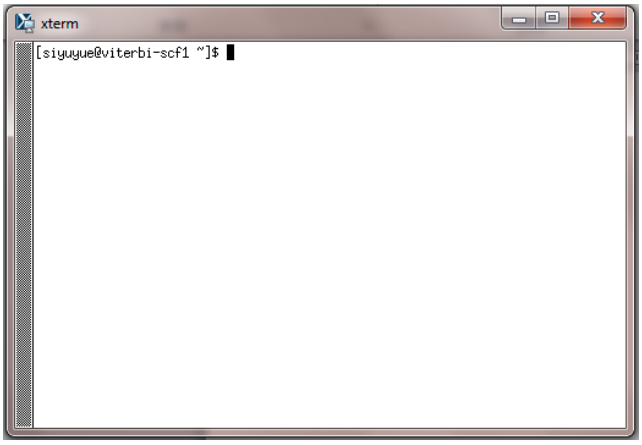
Connection Name: (anything you like)
Host: viterbi-scf1.usc.edu
Login: (your my.usc.edu account name)
Command: /usr/bin/xterm
Password: (your my.usc.edu account password)



Save your connection. Launch it:

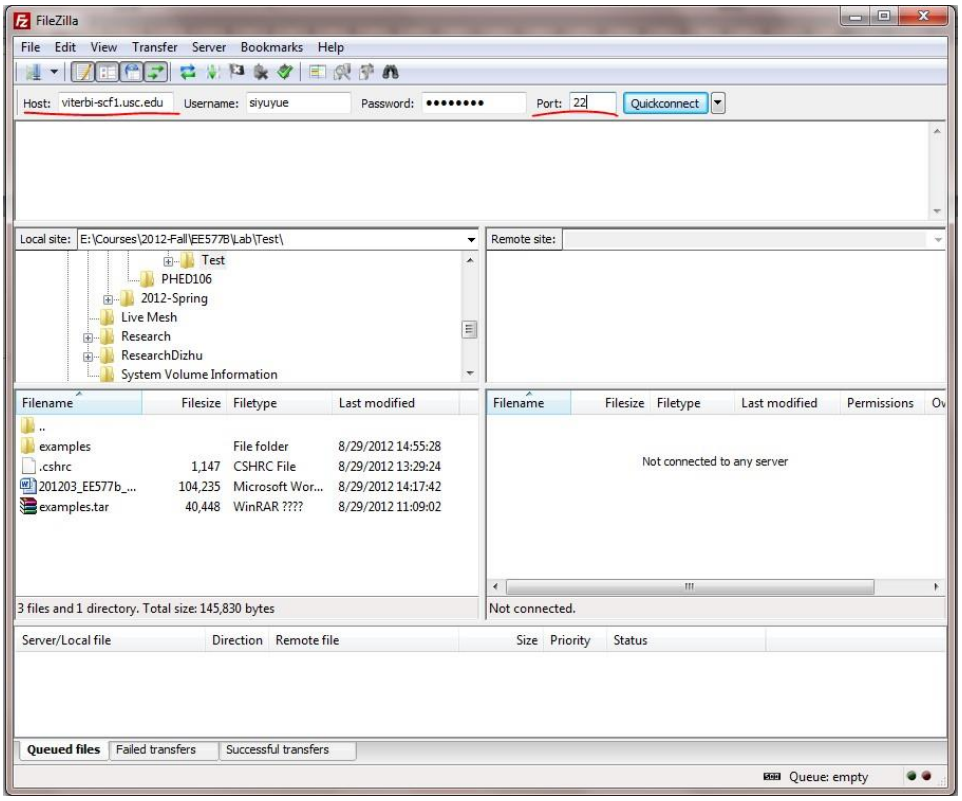


If you see the xterm window like below, congratulations your X-Win32 is all setup.

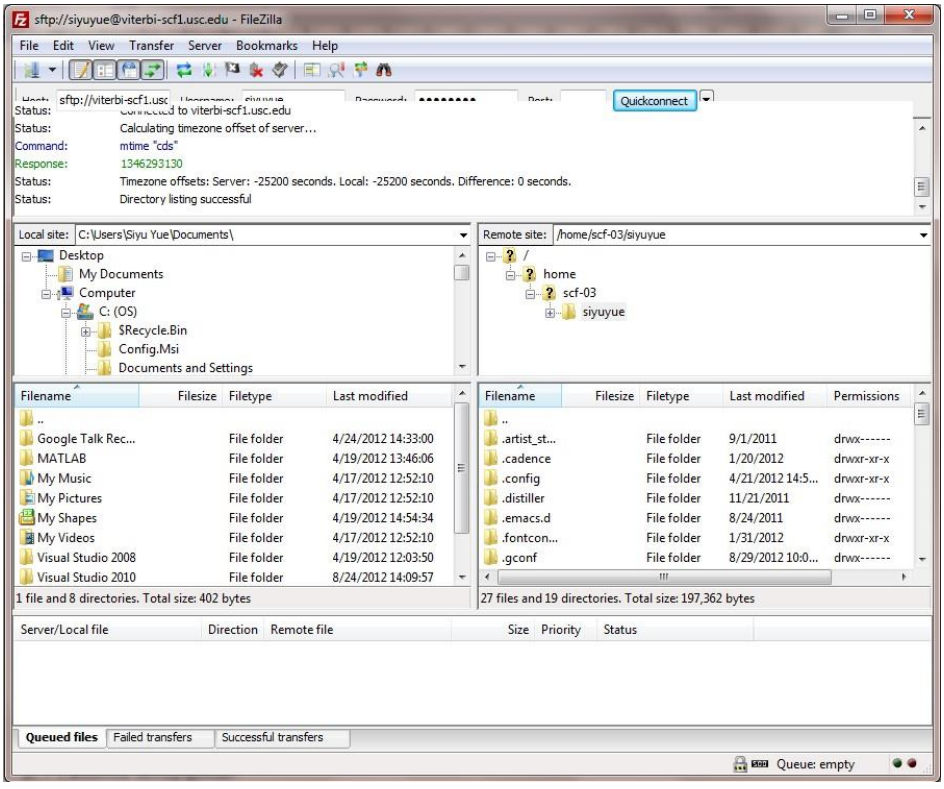


b) Filezilla Connection Setup

Open Filezilla, use **viterbi-scf1.usc.edu** as host and **22** as Port. The username and password are the same as your X-Win32 connection.



Navigate and choose files from the left window to upload and files from the right window to download.



Cadence setup

Before you start, familiarize yourself with the following linux commands:

ls	**// List files**
pwd	**// Show your current directory**
cd	**// Navigate to some directory**
mv	**// Move**
cp	**// Copy**
rm	**// Remove**
mkdir	**// Create a directory**

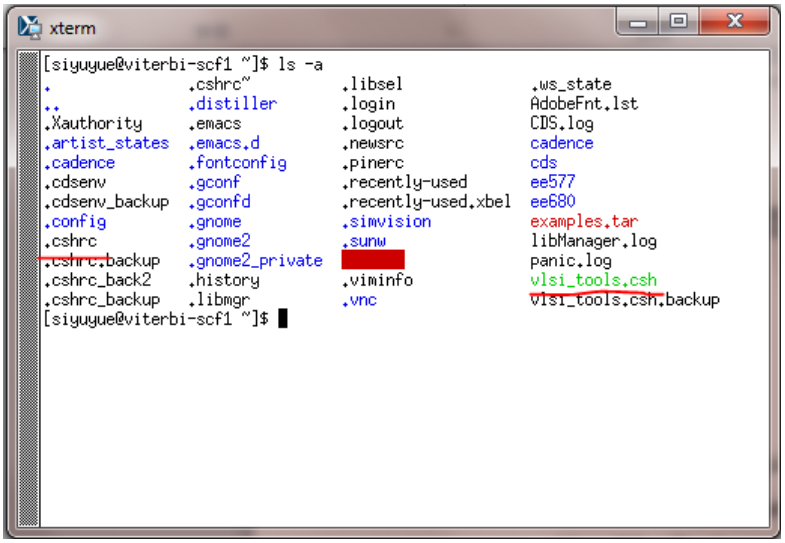
Google them for more information about their usage if needed.

You can find 'cshrc_linux' ,tsmc.spice and 'vlsi_tools.csh' from http://bits.usc.edu/ee209/ site. Note that the file entitled 'cshrc_linux' should be renamed to '.cshrc' after uploading it in your home directory.

Download *.cshrc, tsmc.spice* and *vlsi_tools.csh* from http://bits.usc.edu/ee209/ under Lab Tutorial. Use Filezilla (or scp) to upload these files to your home folder on viterbi-scf1. Make sure they are named .cshrc or vlsi_tools.csh exactly.

Type command "ls –a" to list all files under your home directory:

ls -a



If you need to edit the linux files, don't edit them by Window based editor (e.g., Word, Text). You have to use unix editors, such as gedit, vi, emacs..

If you need to rename those files to .cshrc or vlsi_tools.csh, use command "mv", for example, to rename cshrc to .cshrc, you can say:

mv cshrc .cshrc

Convert the encoding of those two files by dos2unix command:

dos2unix .cshrc

dos2unix vlsi_tools.csh

Create a folder named cds:

mkdir cds

Copy useful files to your cds directory:

cp ~ee577/design_pdk/tsmc25/files/* ./cds/

cp ~ee577/design_pdk/tsmc25/files/.cds* ./cds/

Check you have the following files in the cds folder:

ls -a ./cds/

.cdsinit // cadence initialized file

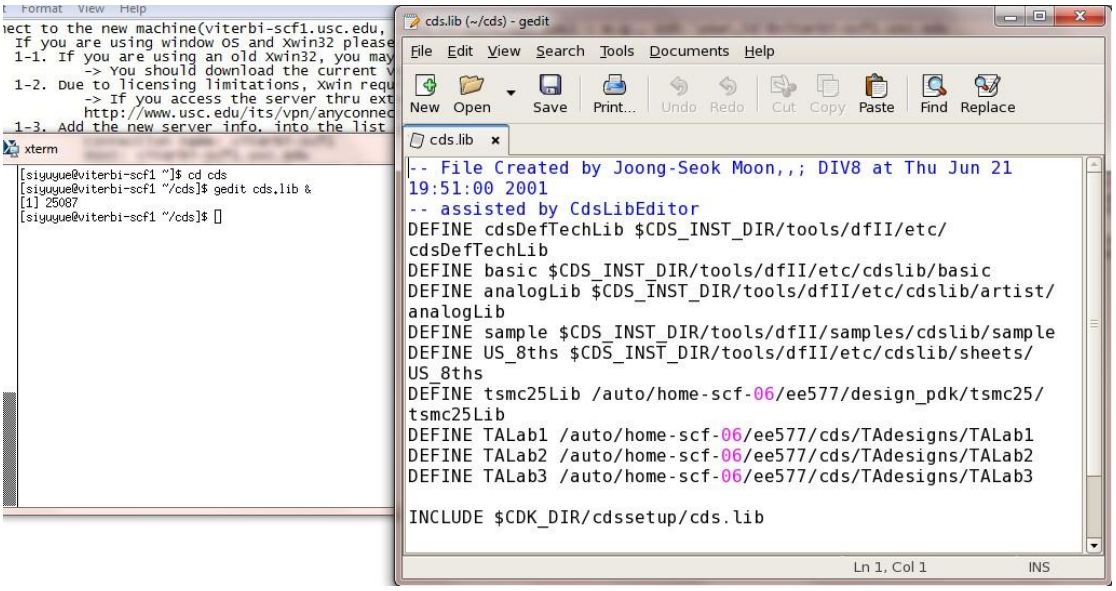
.cdsplotinit	// cadence printing setup file
cds.lib	// cadence library setup file
schBindKeys.il	// Binding key files for shortcut keys
tsmc25.spice	// TSMC 25 spice parameters
leBindKeys.il	// Binding key files for shortcut keys

Now go to the cds folder:

cd cds

~~Use gedit to open cds.lib:~~ This step is no more necessary

~~gedit cds.lib~~



~~Add the following line to it; do not remove any existing content:~~

~~INCLUDE $CDK_DIR/cdssetup/cds.lib~~

Or you can you type 'cd ~', whenever going back to home directory

Go back to your home directory:

cd ..

Copy the cadence environment files to your cds working directory:

cp ~ee577/design_pdk/ncsu-cdk-1.6.0.beta/cdssetup/cdsinit ./cds/.cdsinit

Copy the .simrc file to your cds directory:

cp ~ee577/design_pdk/ncsu-cdk-1.6.0.beta/cdssetup/simrc ./cds/.simrc

Then you can source .cshrc file:

source .cshrc

If nothing comes out, then you're successful:

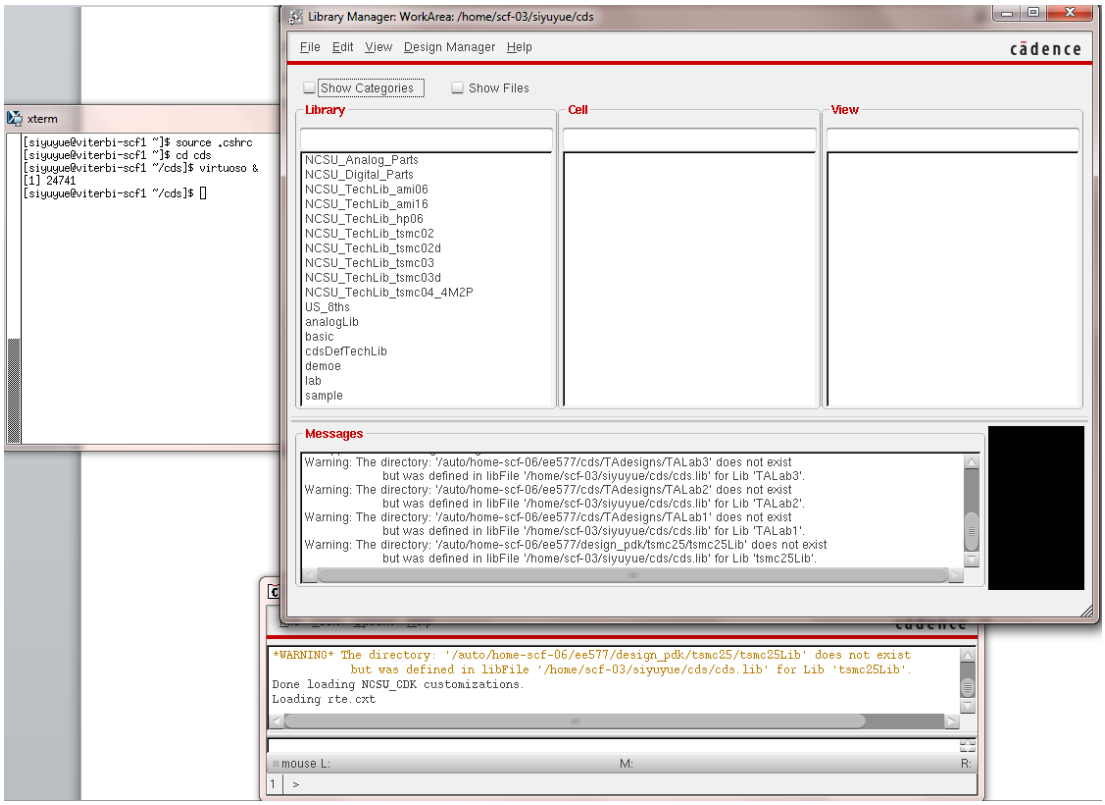
Please remember that you need to source .cshrc every time you login before running virtuoso. You don't need to repeat other steps though.

To run virtuoso, now go to cds directory: (*always run virtuoso in the cds directory*)

cd cds

And open virtuoso: (by adding **&** you can use virtuoso and xterm and the same time)

virtuoso &



Make sure you can see those NCSU_XX libraries and then you're all set!

.cdsplotinit	// cadence printing setup file
cds.lib	// cadence library setup file
schBindKeys.il	// Binding key files for shortcut keys
tsmc25.spice	// TSMC 25 spice parameters
leBindKeys.il	// Binding key files for shortcut keys

A. Make sure you can run cadence tool by typing.

%**which virtuoso**

/usr/usc/cadence/2009/IC610/tools/dfII/bin/virtuoso

B. Go to your home directory, open your .cshrc file and add the following lines at the end of this file:

setenv CDK_DIR /home/scf-06/ee577/design_pdk/ncsu-cdk-1.6.0.beta

setenv CDS_Netlisting_Mode Analog

C. Close the .cshrc file and source this file by typing the following command:

% **source .cshrc**

D. Open the library file cds.lib which is located in your cds directory. Just add the following line to cds.lib. Do not remove existing contents in cds.lib:

INCLUDE $CDK_DIR/cdssetup/cds.lib

E. Go to your home directory. Copy the cadence environment files to your cds working directory by typing the following command while you are in your home directory:

%**cp ~ee577/design_pdk/ncsu-cdk-1.6.0.beta/cdssetup/cdsinit ./cds/.cdsinit**

F. Stay at your home directory. Copy the .simrc file in your cds directory by typing the following command while you are in your home directory:

% **cp ~ee577/design_pdk/ncsu-cdk-1.6.0.beta/cdssetup/simrc ./cds/.simrc**

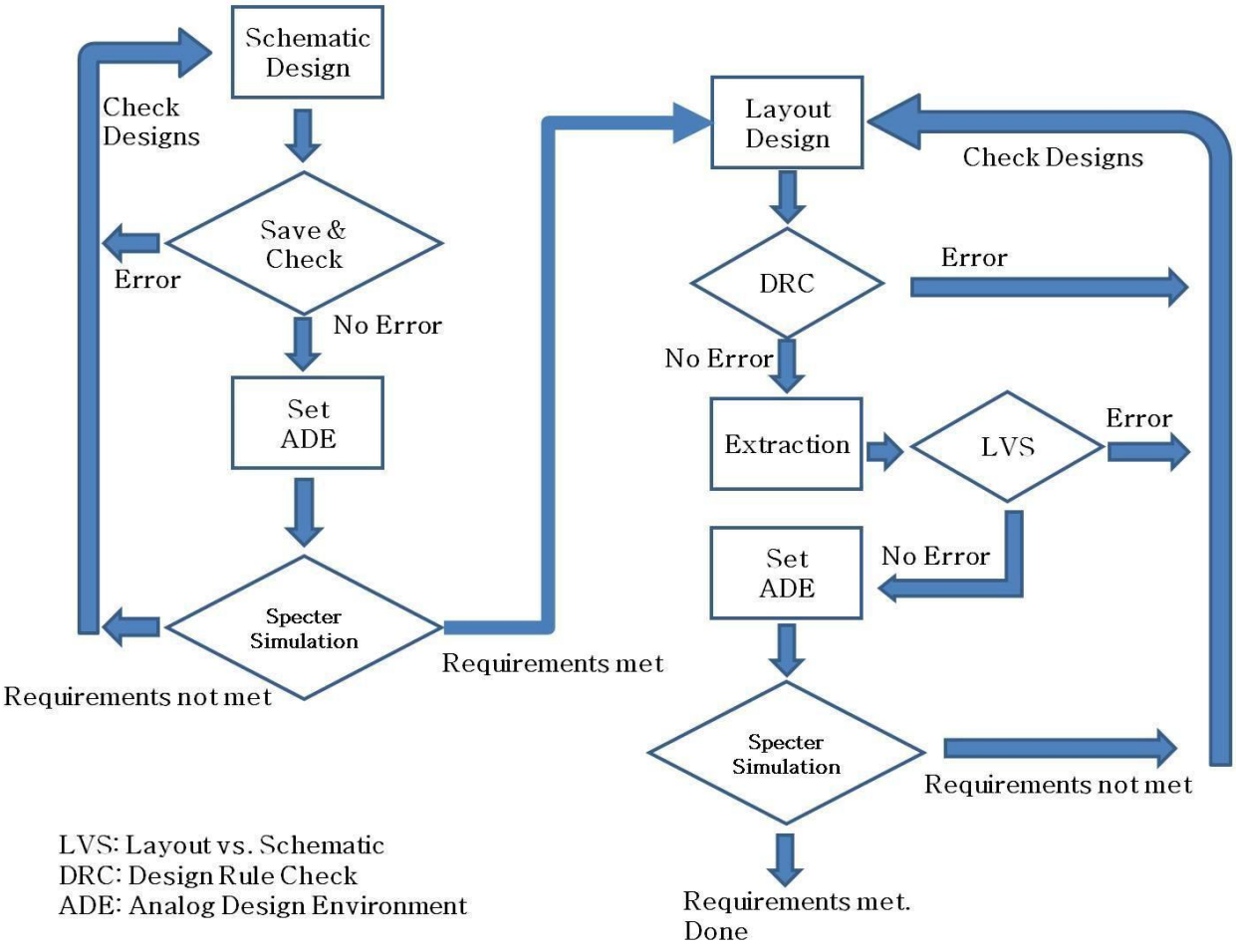
Note that the name of the file that you are accessing is "cdsinit" but you need to save it as ".cdsinit". Also note that you may already have a ".cdsinit" file from the past in your cds directory. In this case you still need to overwrite it by this new file.

G. Always invoke "virtuoso" in your ~/cds directory because all setup files are in this directory. Type **virtuoso &** at the command prompt. The "&" is for background execution, it is useful when we want to keep the command prompt in the same console.

Basic Design Flow

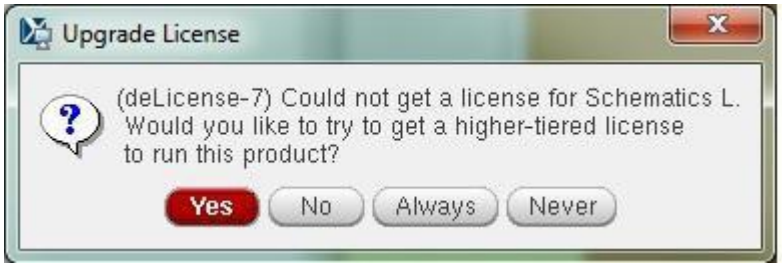
1. Overall design flow

Following flow chart shows overall design flow.

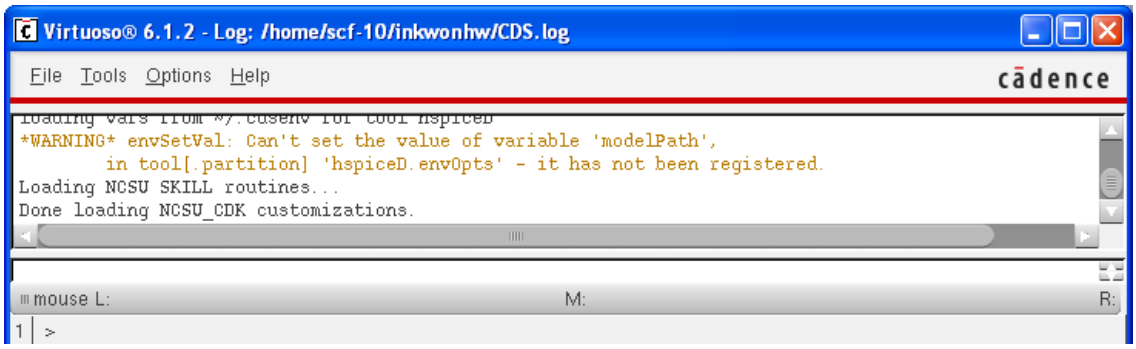


2. Create Library

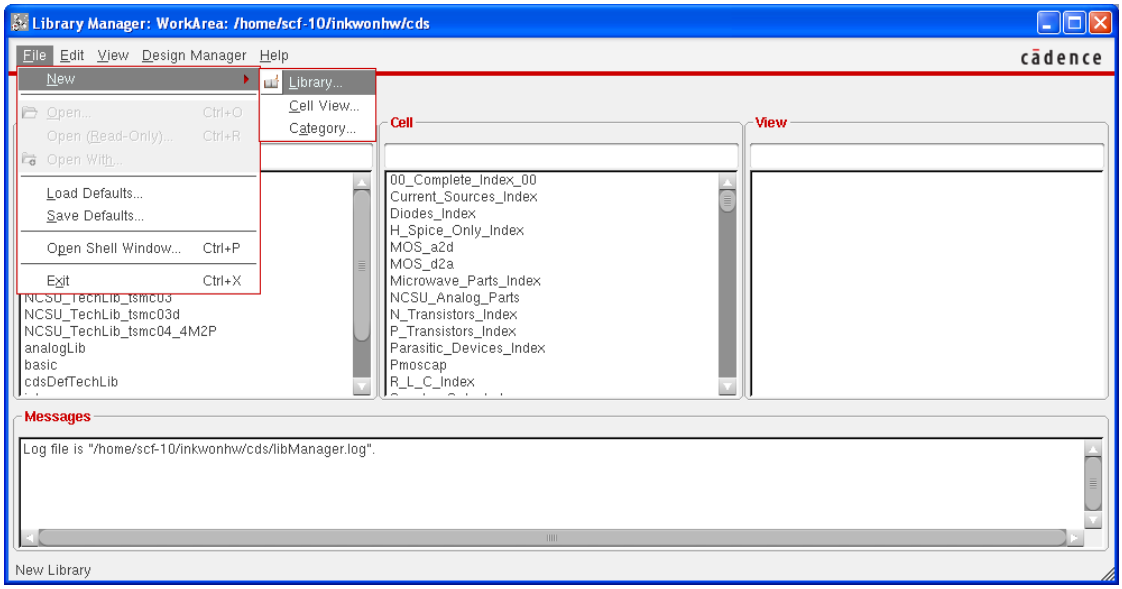
For prompt to access for higher tiered license, click “always”.



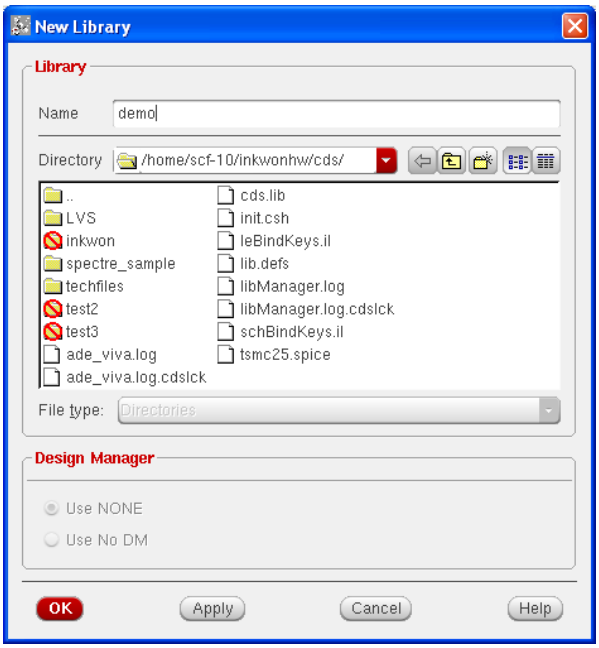
A. Tools → Library Manager

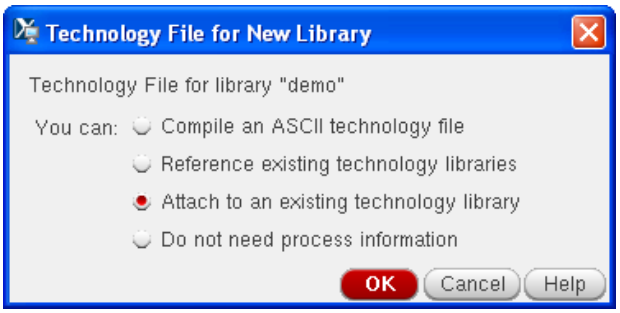


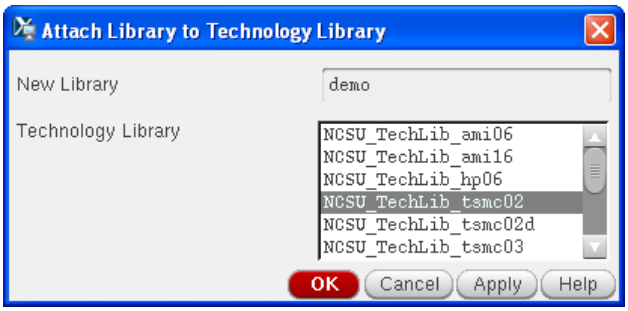
B. File → New → Library



C. Give a name and attach it to a technology library



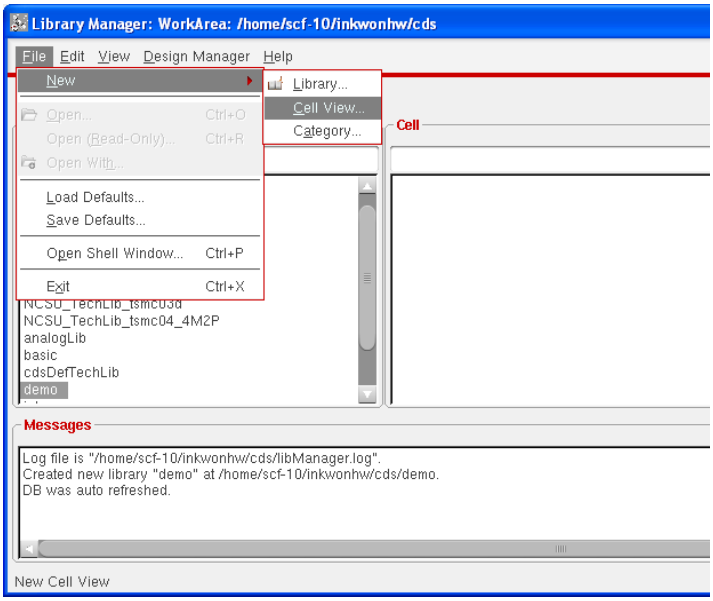


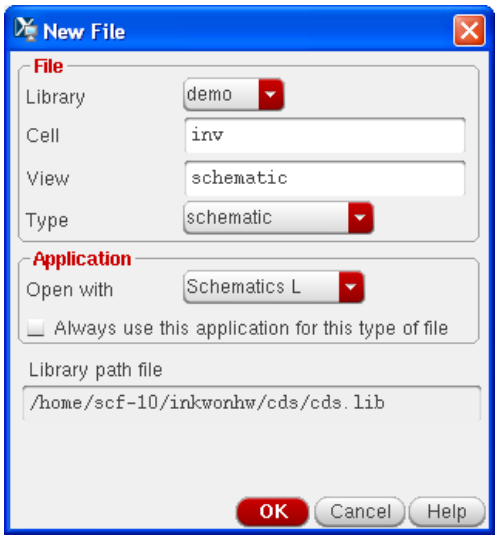


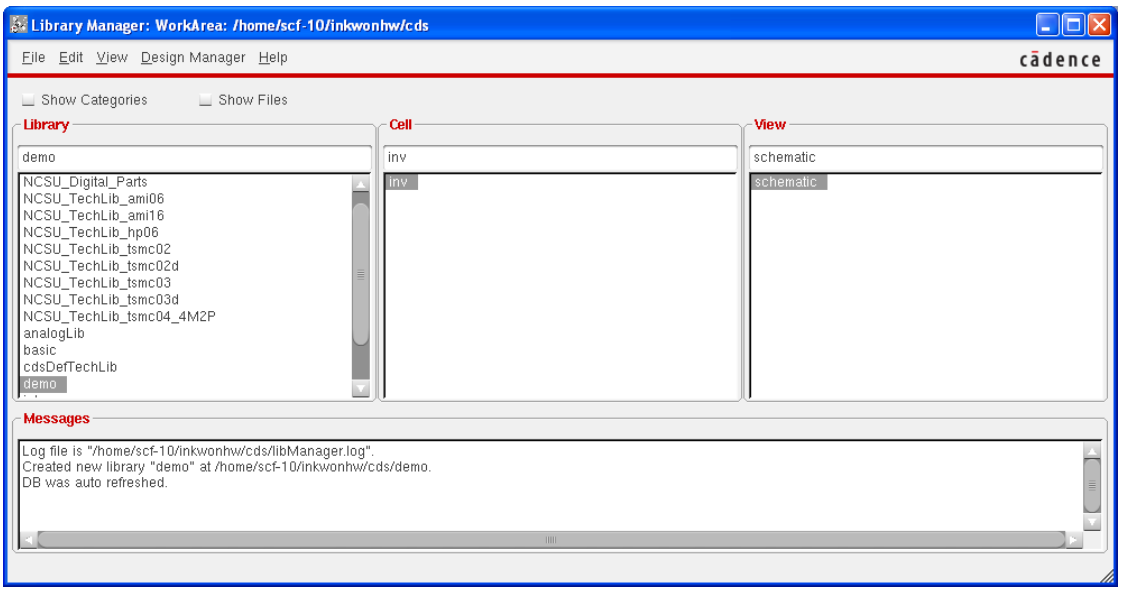
3. Schematic

A. Create a cell view

select the library just created, File->new





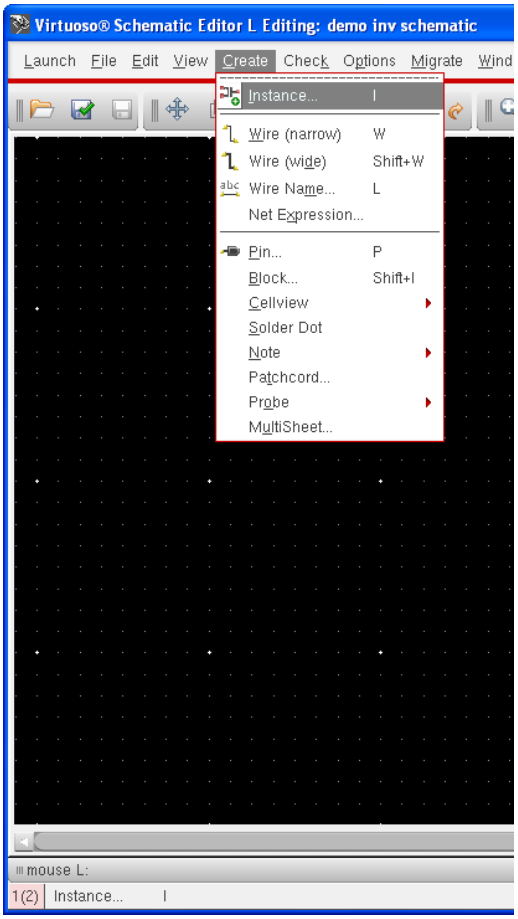


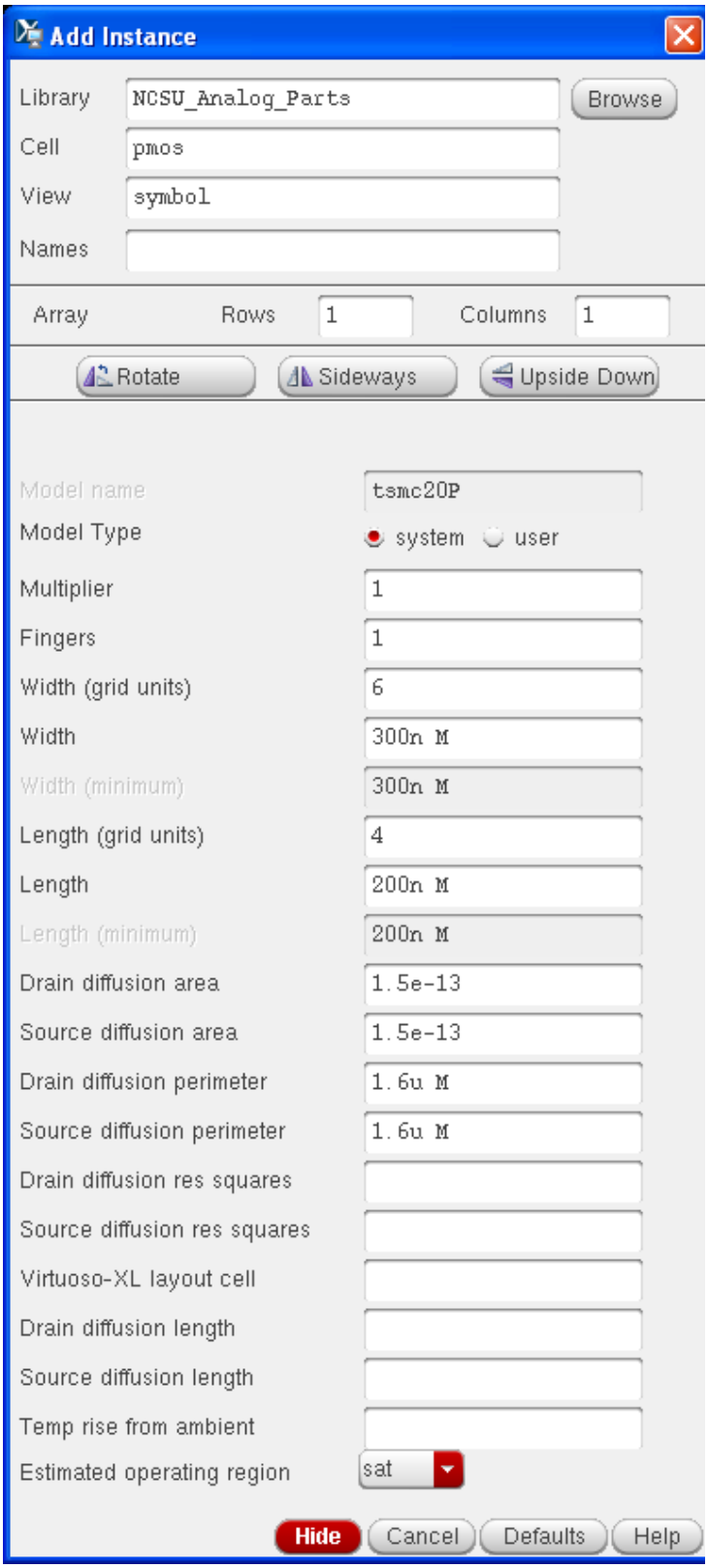
B. Draw a schematic

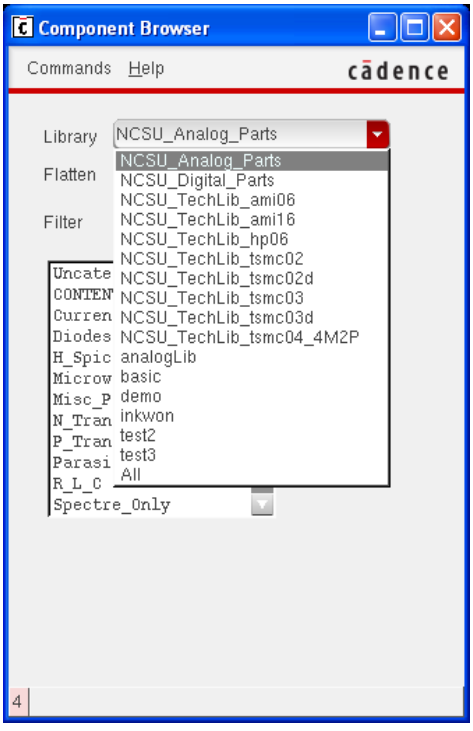
i. Add instances – pmos

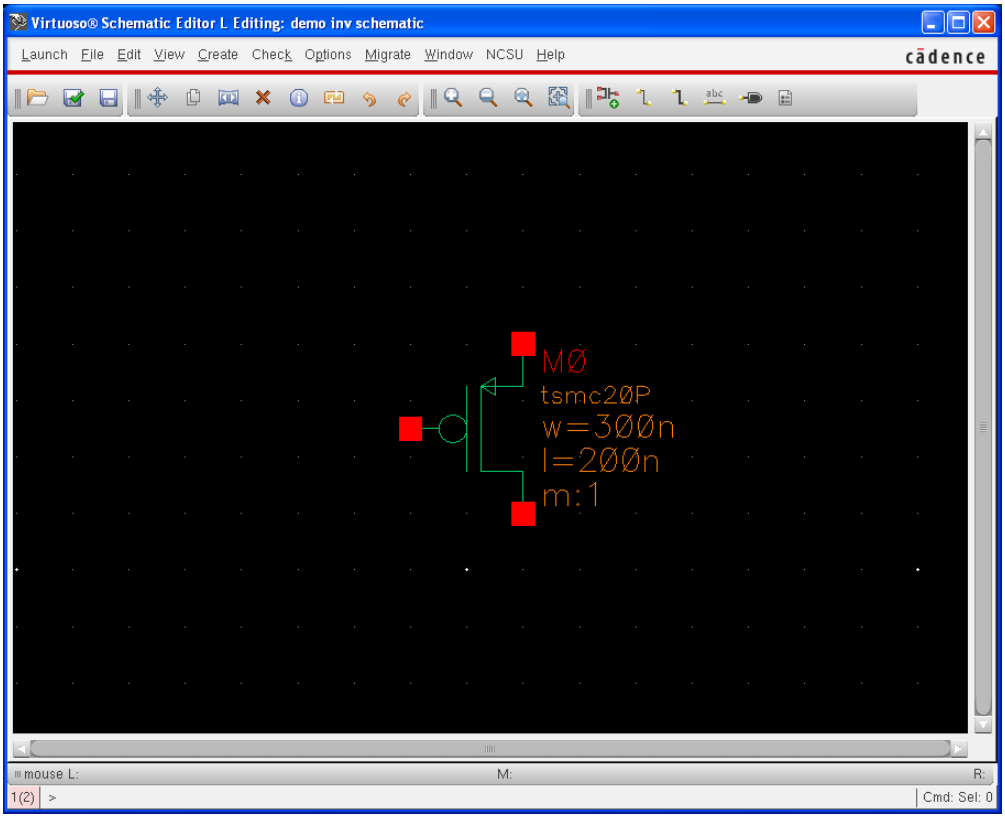
You can modify Width of transistors. Don‟t modify length unless you have a special purpose.

You should select a NCSU_Analog_Parts library.

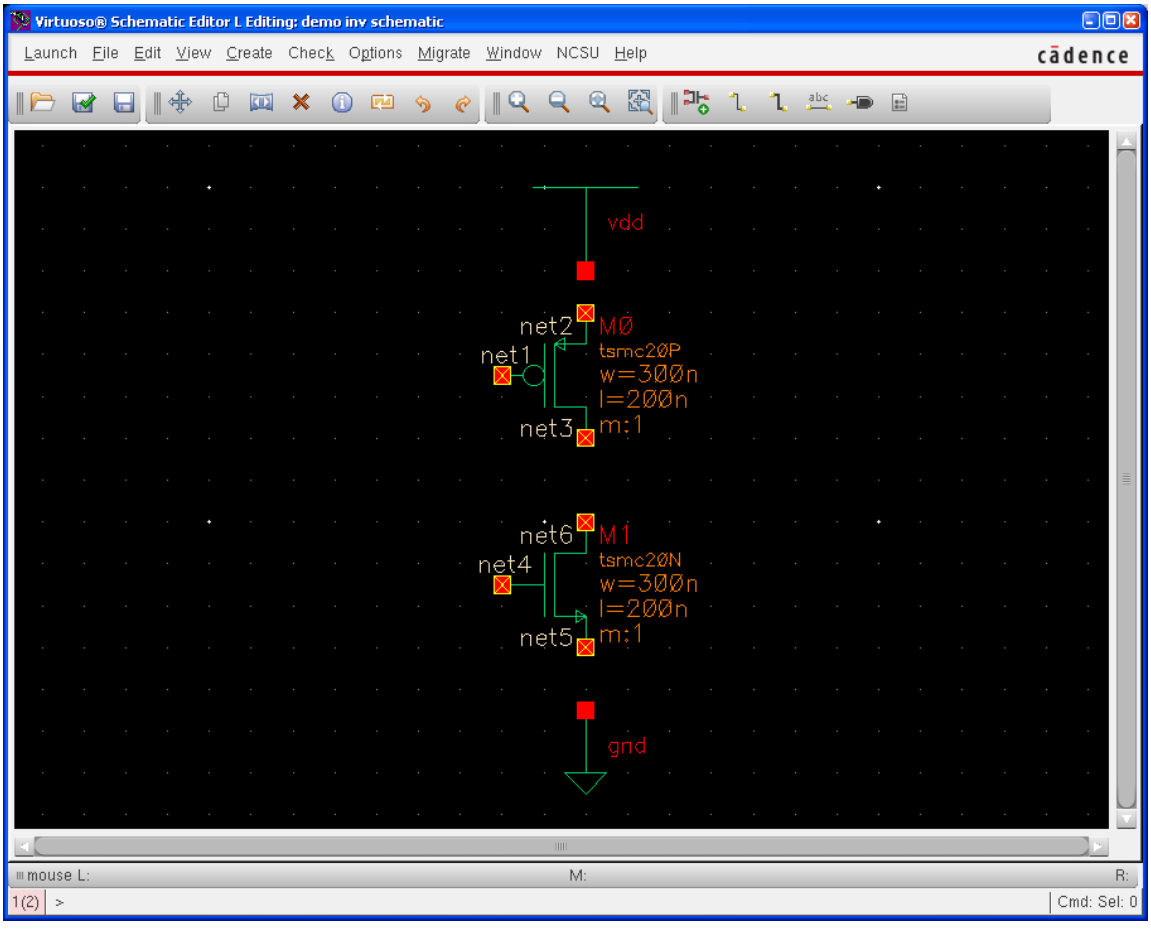




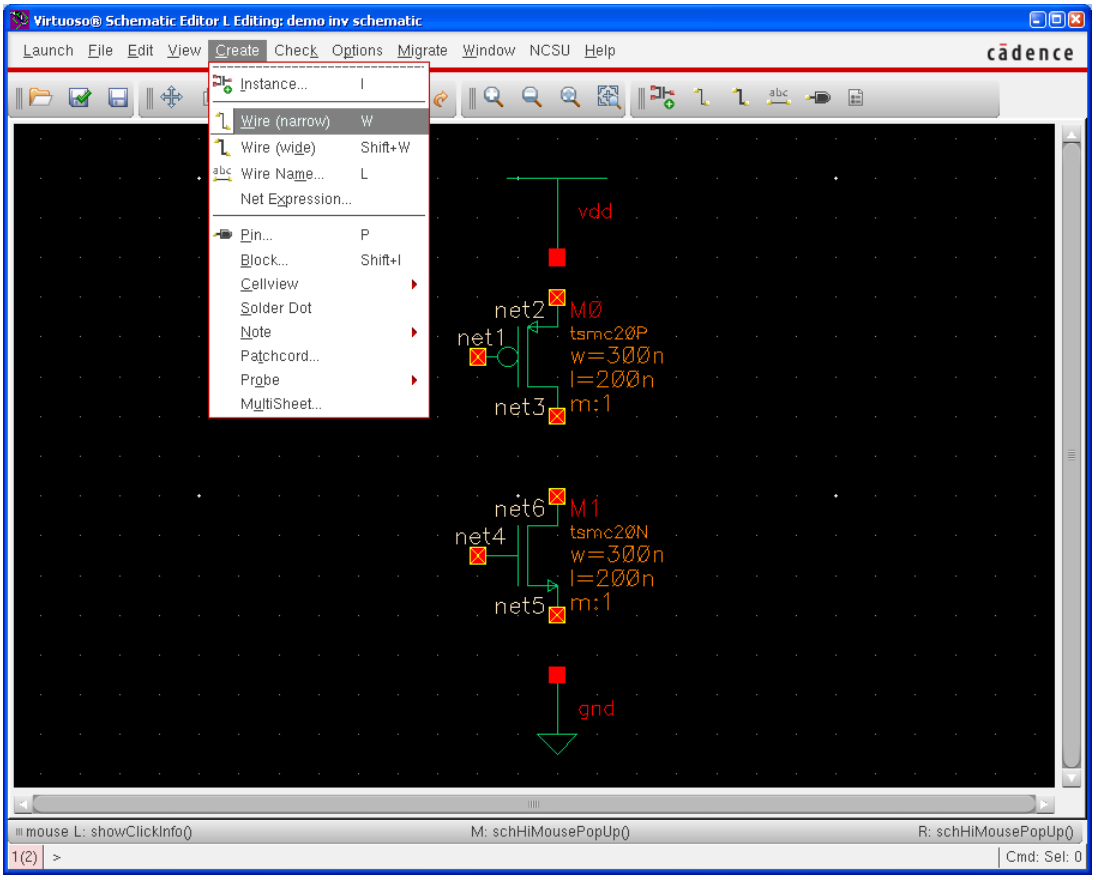


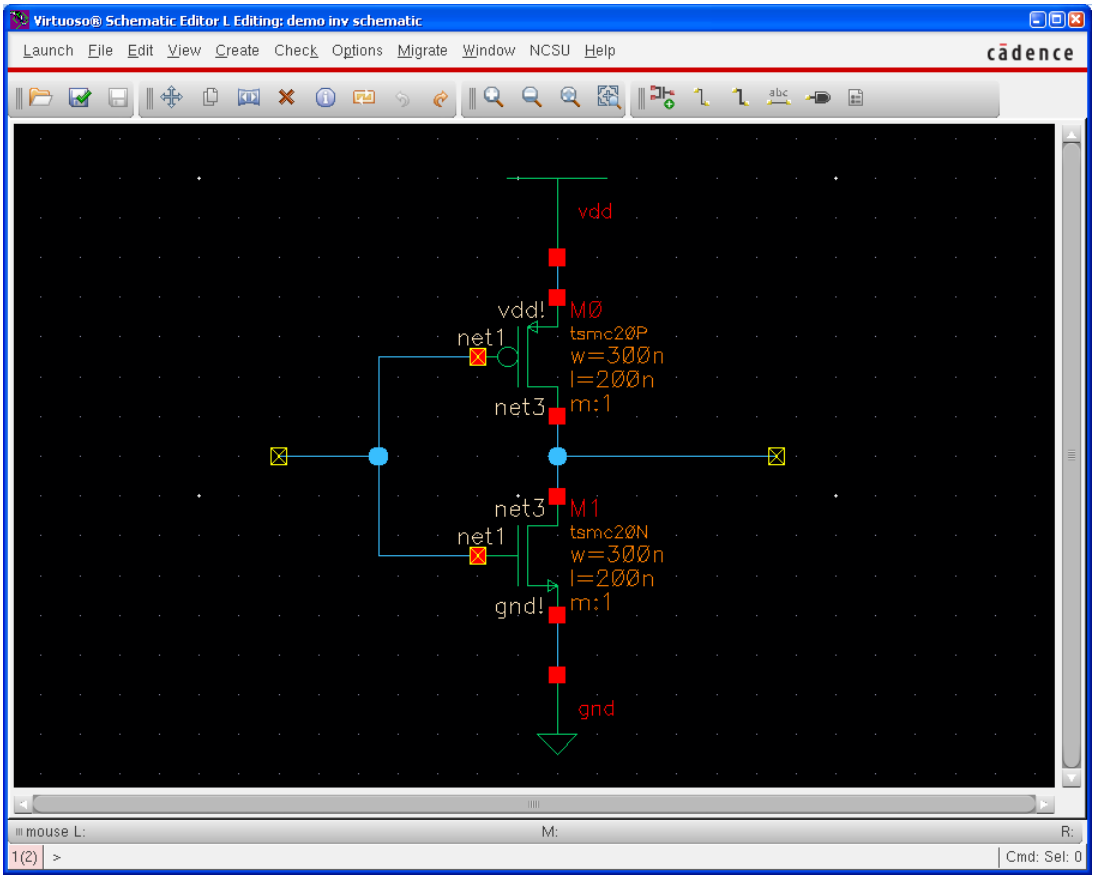


ii. Add instances – nmos, vdd, and gnd

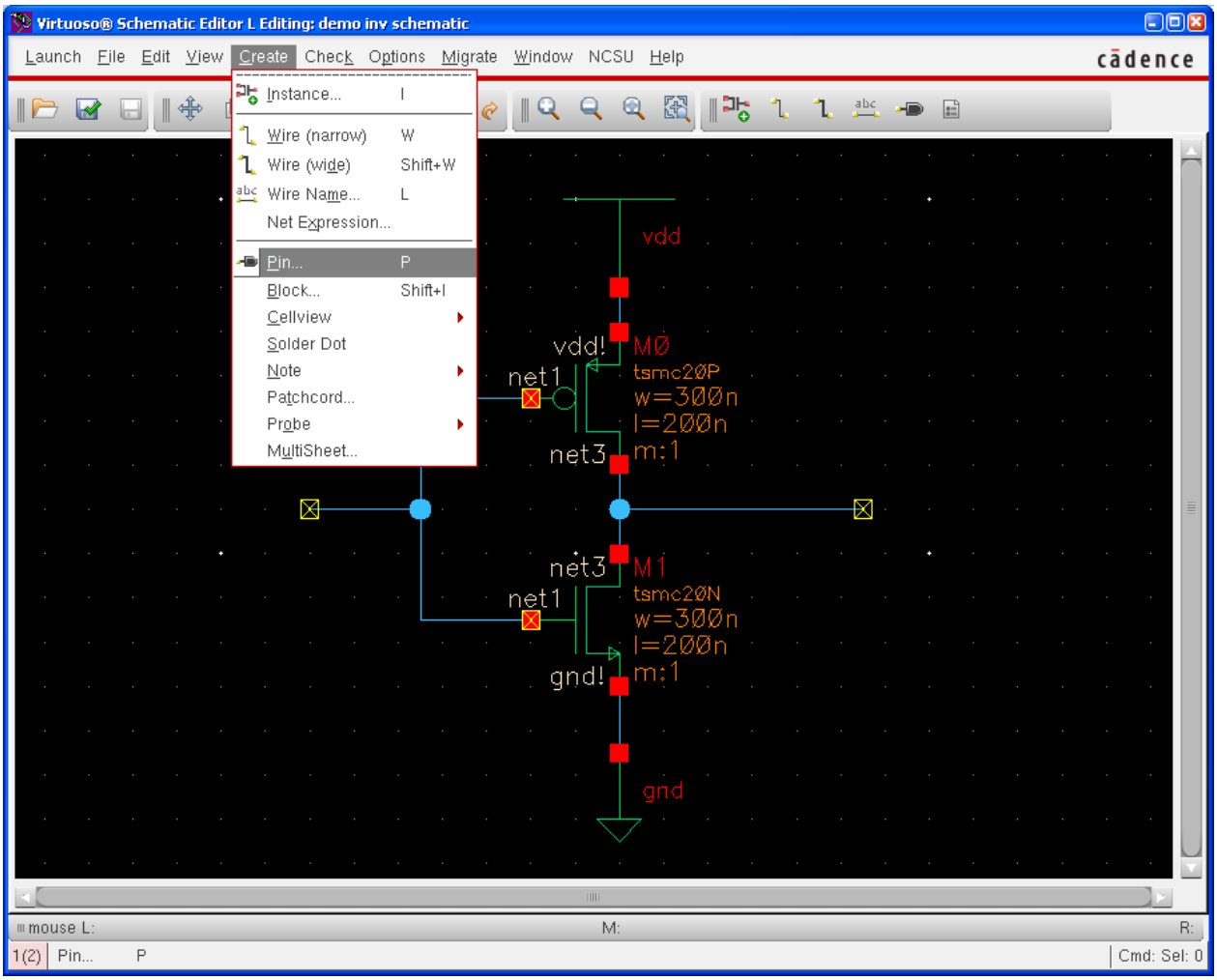


iii. Add wires: Create → Wire

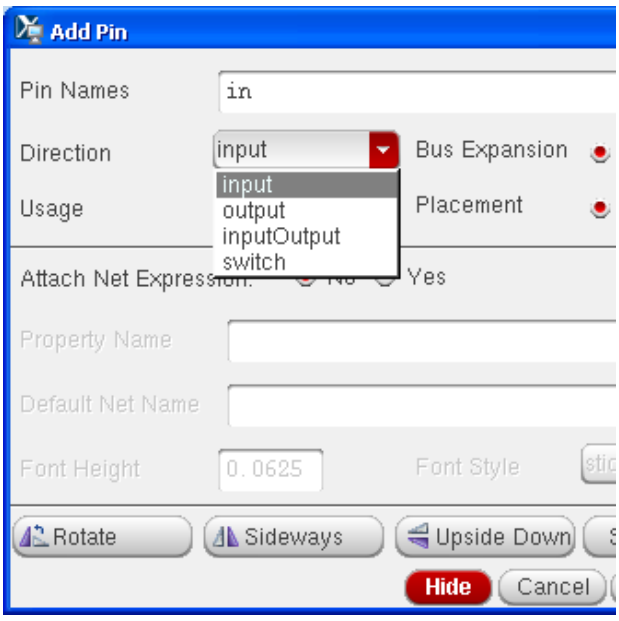


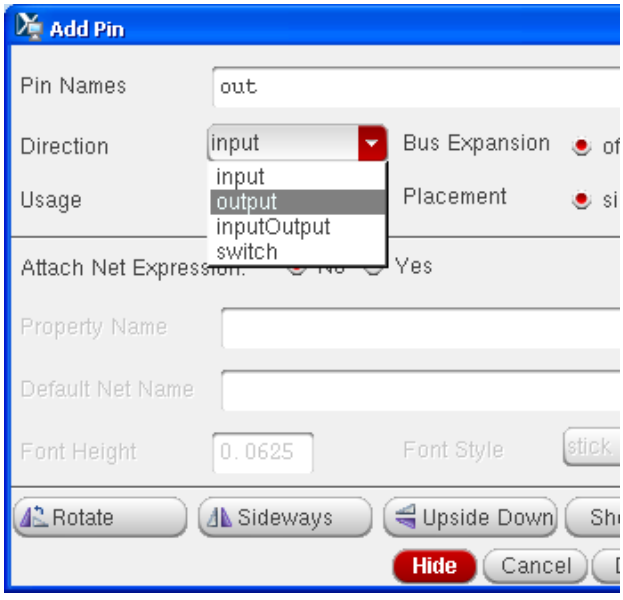


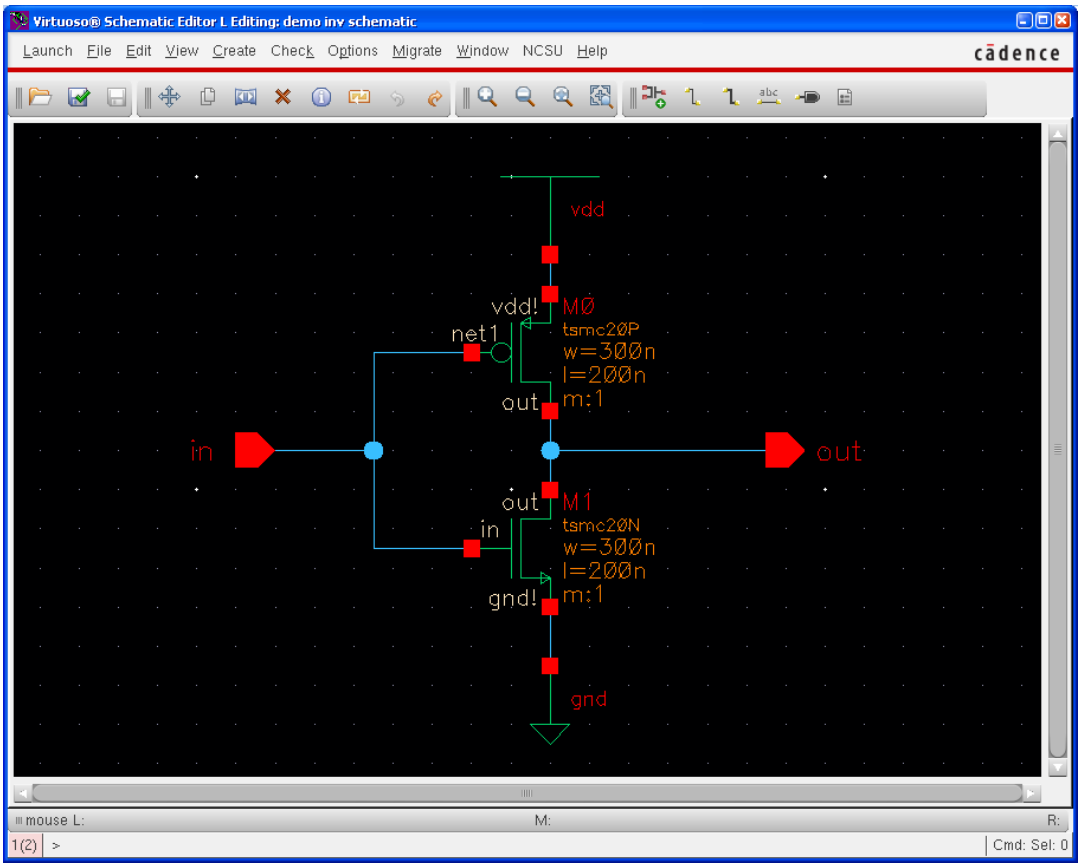
iv. Add pins: Create → Pin



We have for different types of direction. For schematics, we only use two types, input and output. InputOutput type is for supply changes, and it is necessary only for layout. We will discuss about this later.





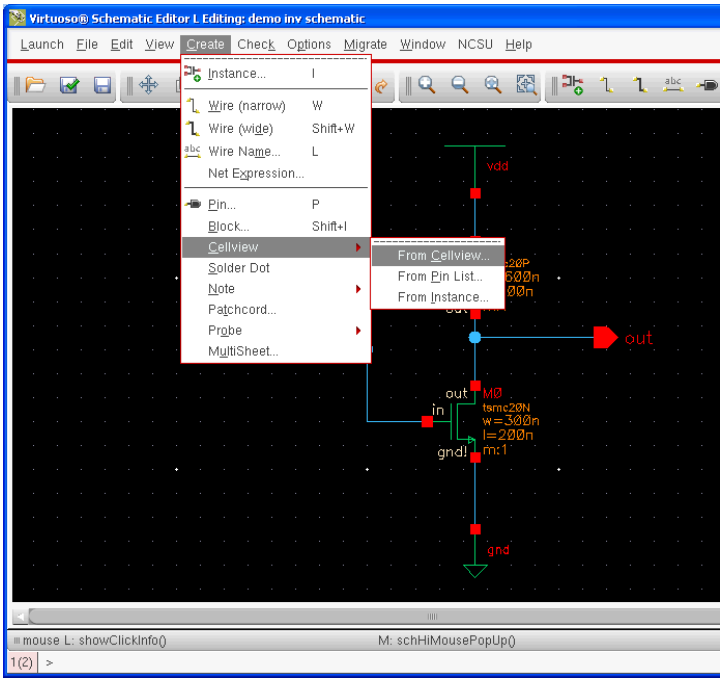


Check and save →  to make sure there are no errors.

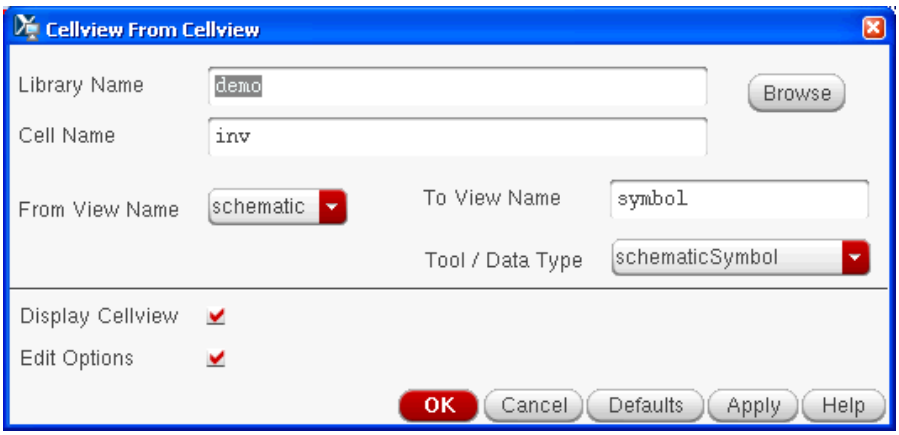
Now, we completed a schematic design.

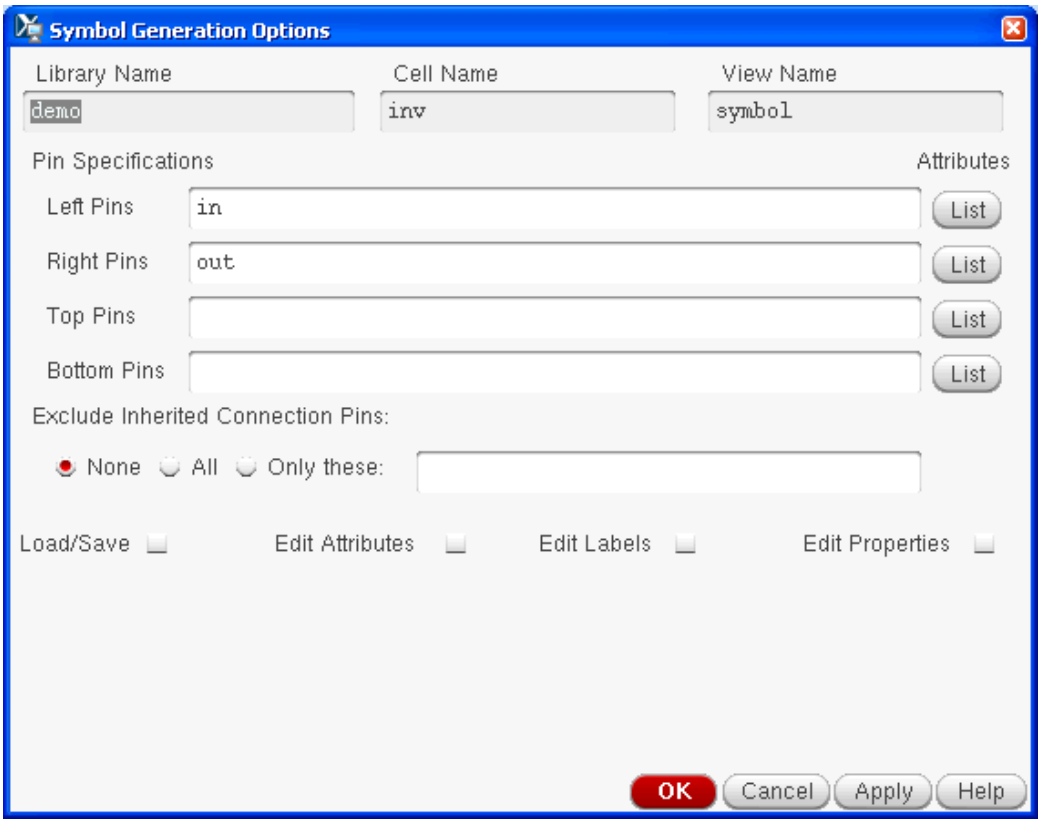
C. Create a symbol (Optional)

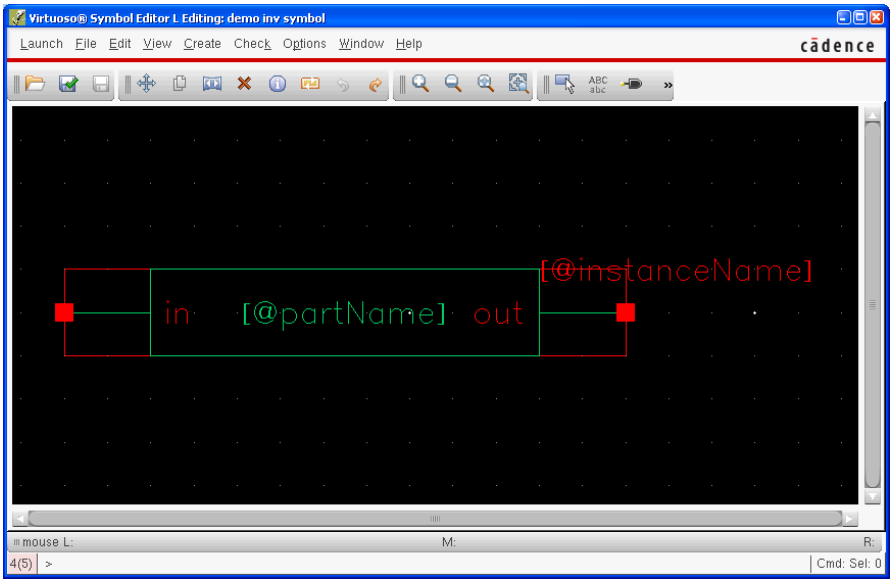
For hierarchical design, we may need to make symbols of designed circuits.



Create → CellView → From Cellview


Cellview From Cellview
Library Name
demo
Browse
Cell Name
inv
From View Name
schematic
To View Name
symbol
Tool / Data Type
schematicSymbol
Display Cellview
Edit Options
OK
Cancel
Defaults
Apply
Help


Symbol Generation Options
Library Name
Cell Name
View Name
demo
inv
symbol
Pin Specifications
Attributes
Left Pins
in
List
Right Pins
out
List
Top Pins
List
Bottom Pins
List
Exclude Inherited Connection Pins:
None
All
Only these:
Load/Save
Edit Attributes
Edit Labels
Edit Properties
OK
Cancel
Apply
Help


Virtuoso® Symbol Editor L Editing: demo inv symbol
Launch File Edit View Create Check Options Window Help
cadence
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[@partName]
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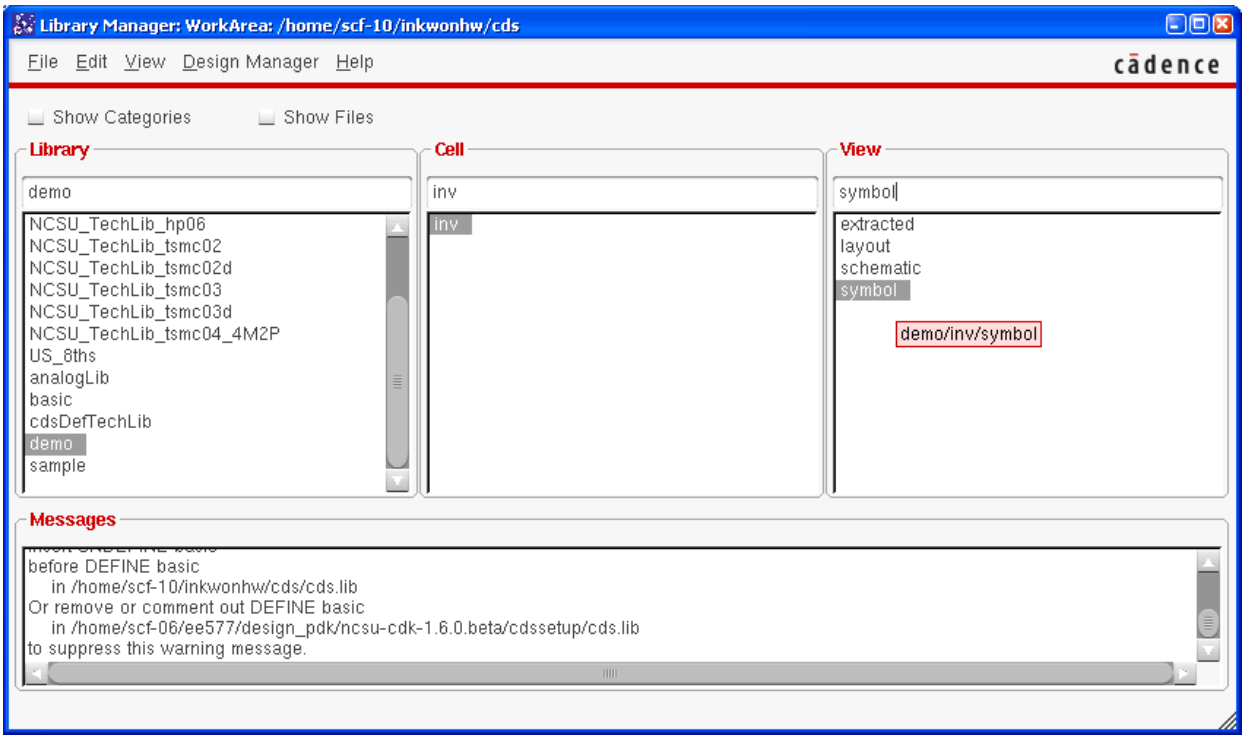


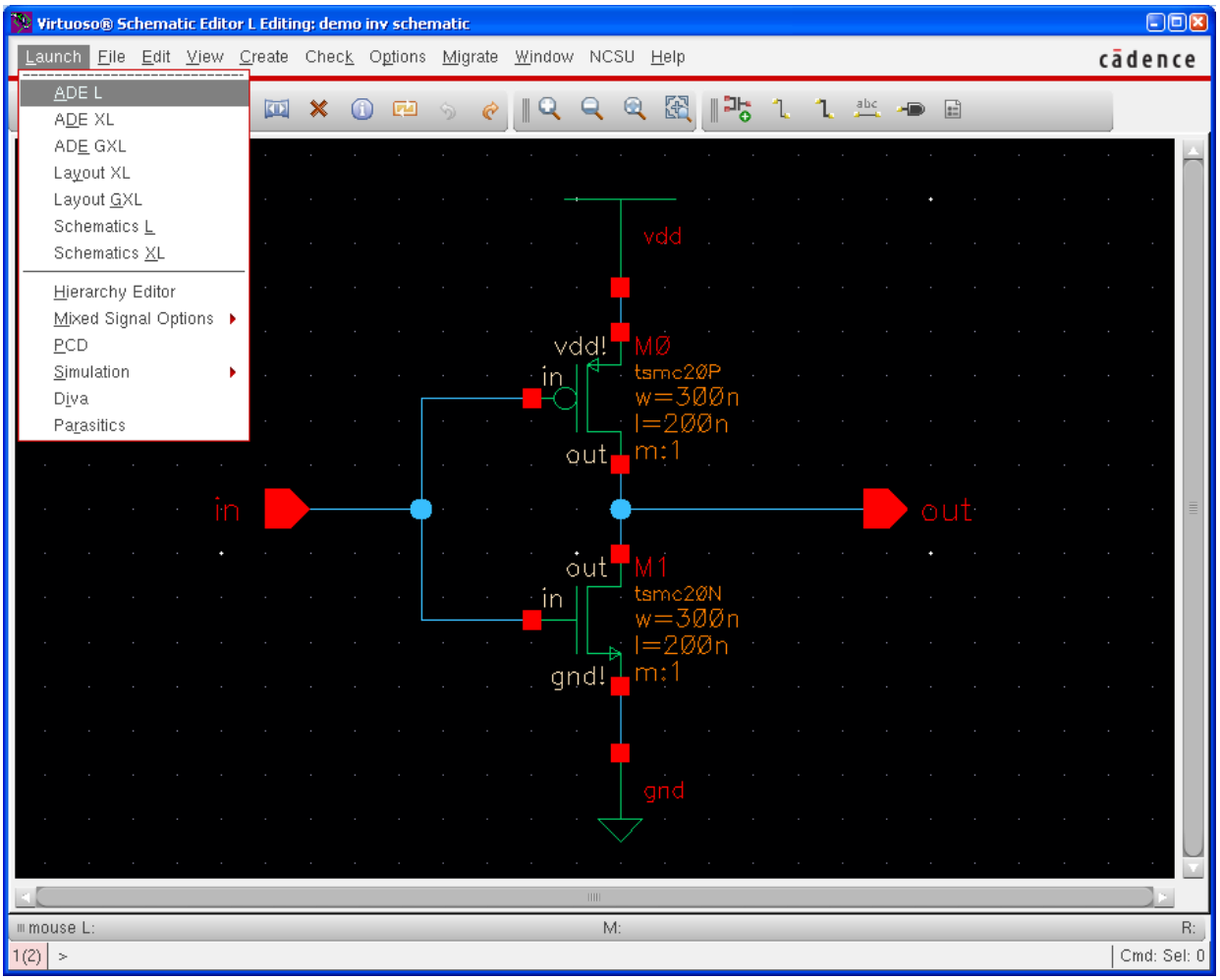
Remember that when you use more than one symbol in schematic, they all will have common Vdd and Gnd even if there are one Gnd and Vdd for each symbol (in the original design). To design with symbols in layout, you should make sure that all of the Vdd and Gnds are connected.

4. Run Spectre simulation (Transient analysis)

We will run spectre simulation. This section is for **both** schematics and layouts. I will show an example for a schematic. You can do the same thing for a layout.

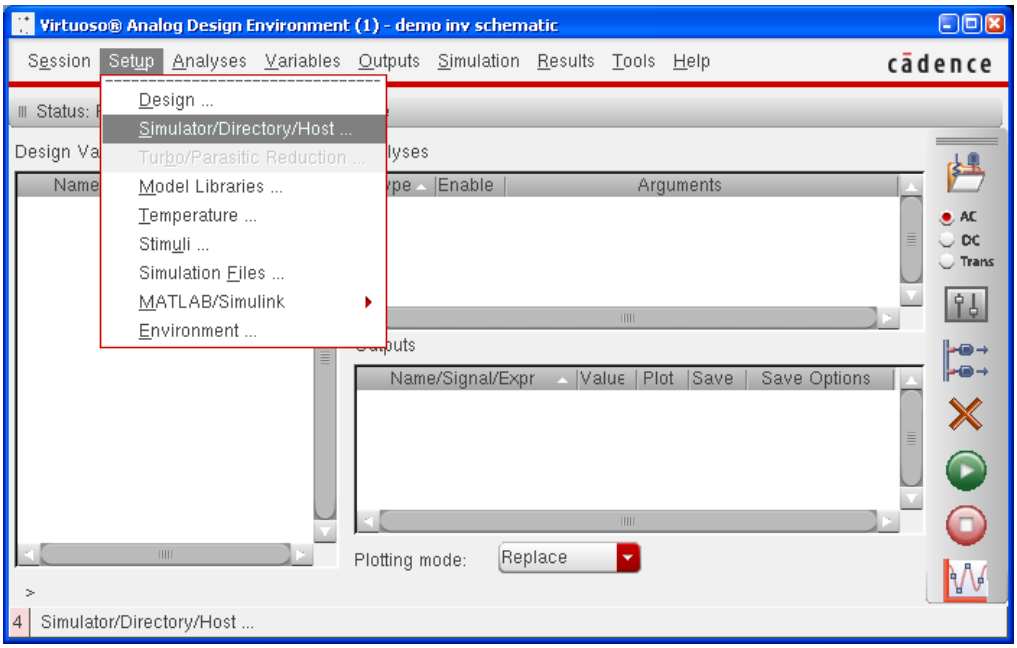
A. Launch ADE (Analog Design Environment) L

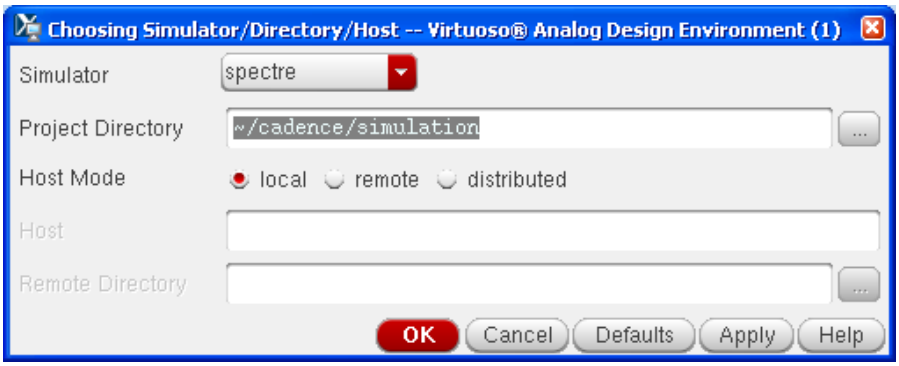
Launch → ADE L



B. Basic setup

Check if your simulator is spectre. You can modify project directory.

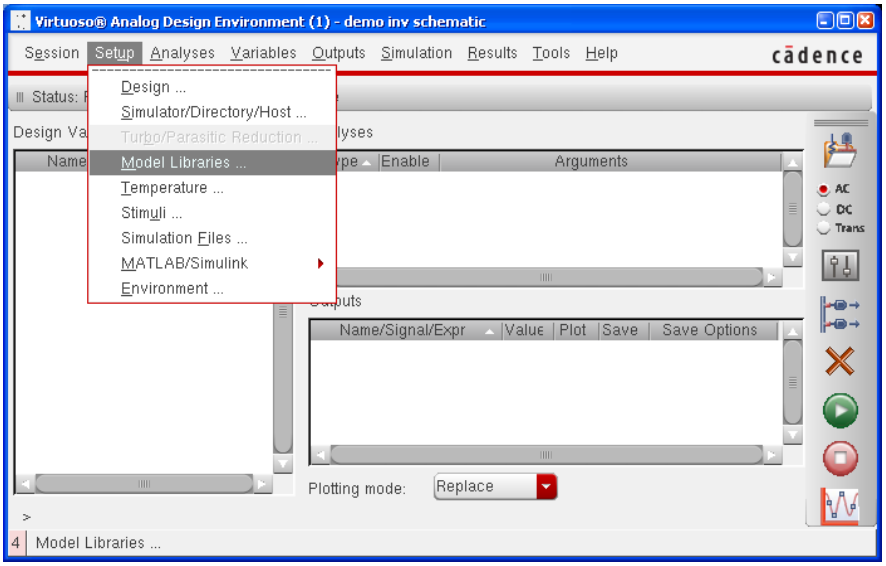


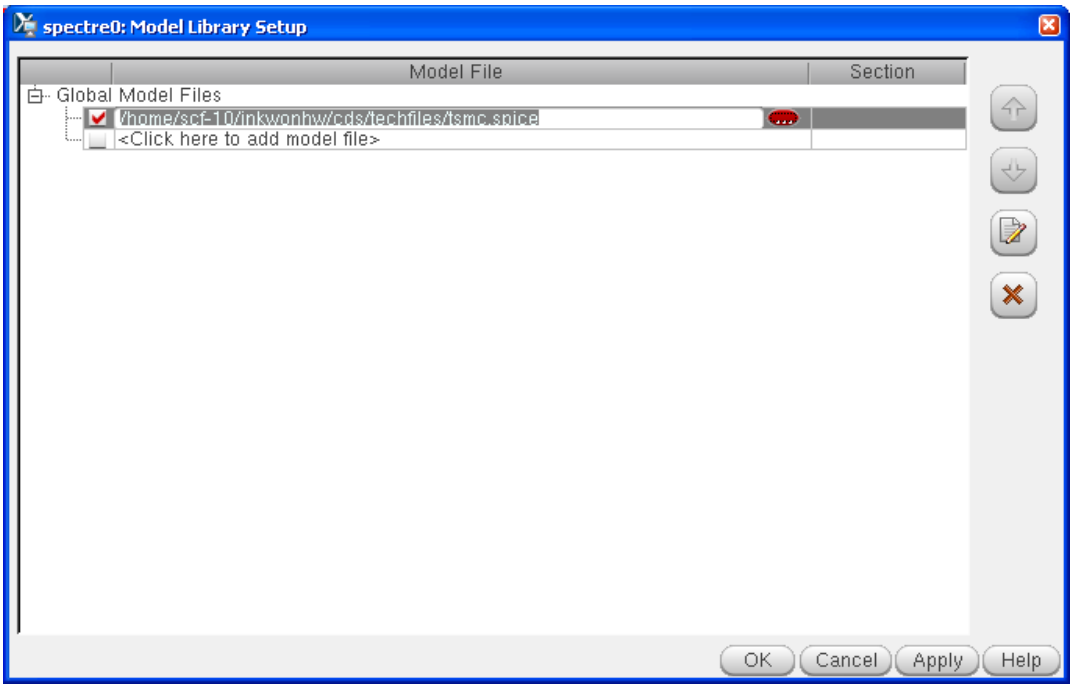


C. Model Libraries

You can download a library file at the DEN blackboard.

Put the tech file under /home/scf-10/your-user-name/cds/techfiles/

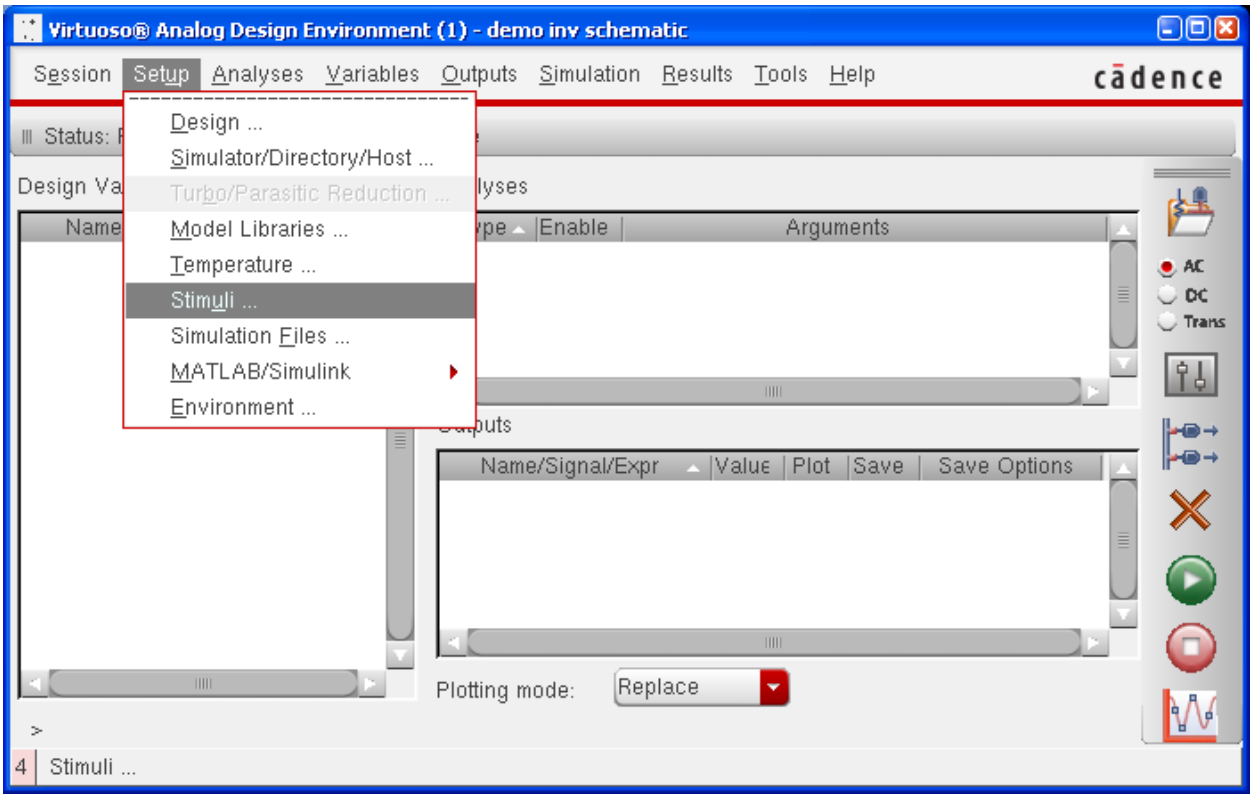




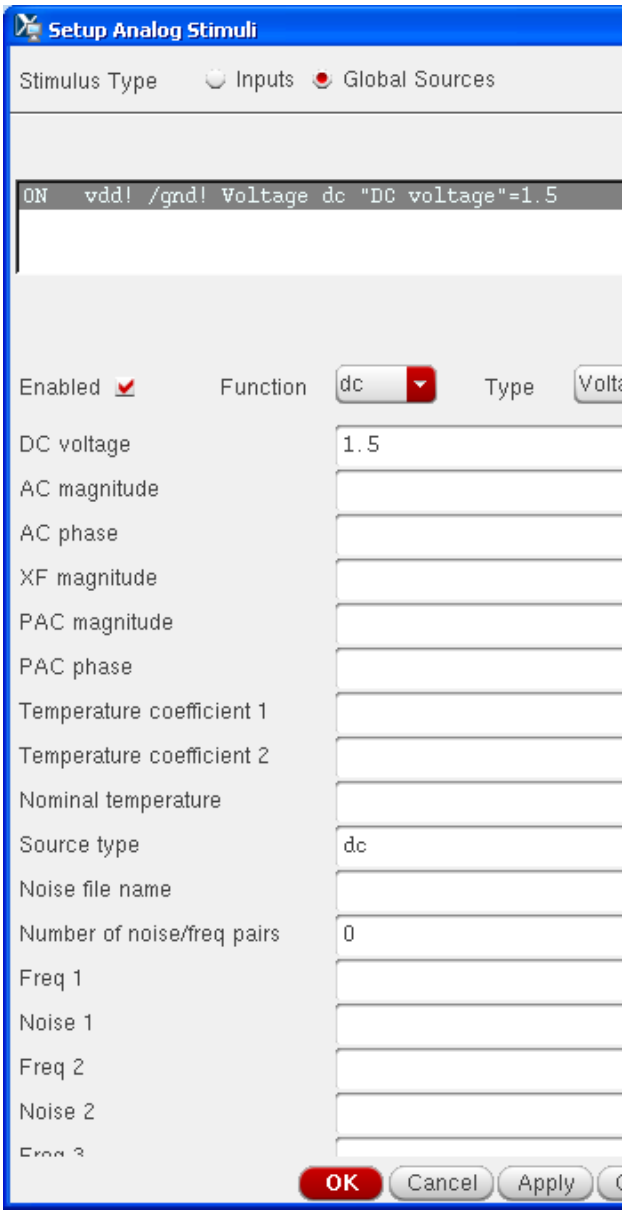
Please only use the provided tsmc file because some tsmc files does not work correctly.

D. Stimuli

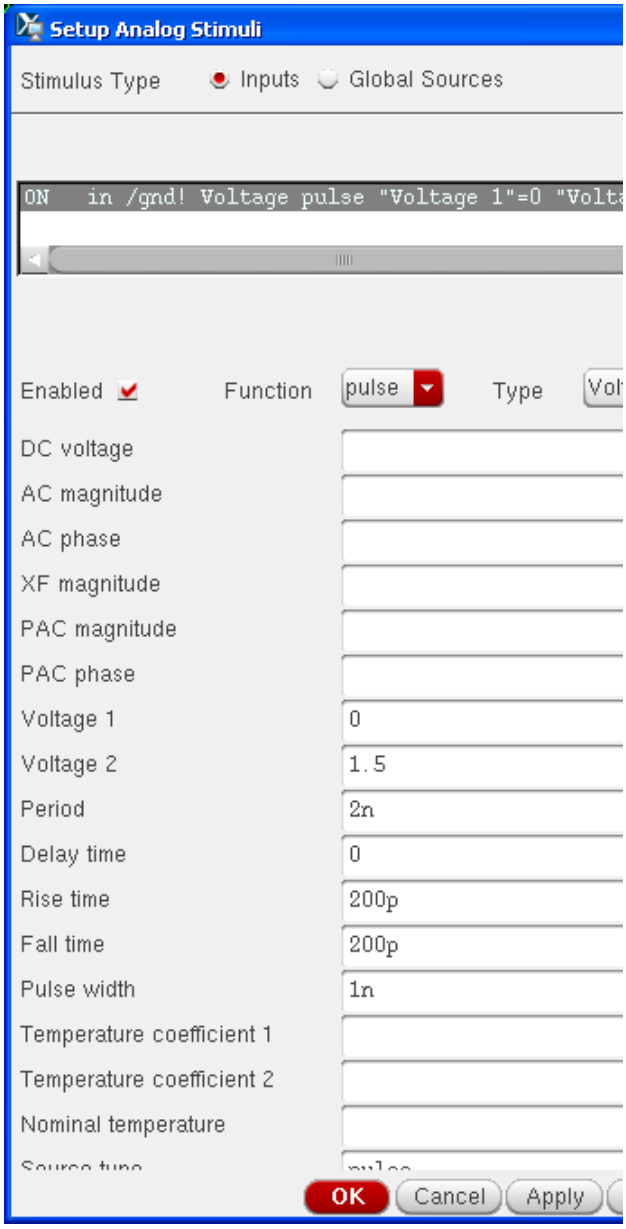
Define input signals include supply nets (for layout, vdd! and gnd! are under inputs and both should be enabled.)



Global sources



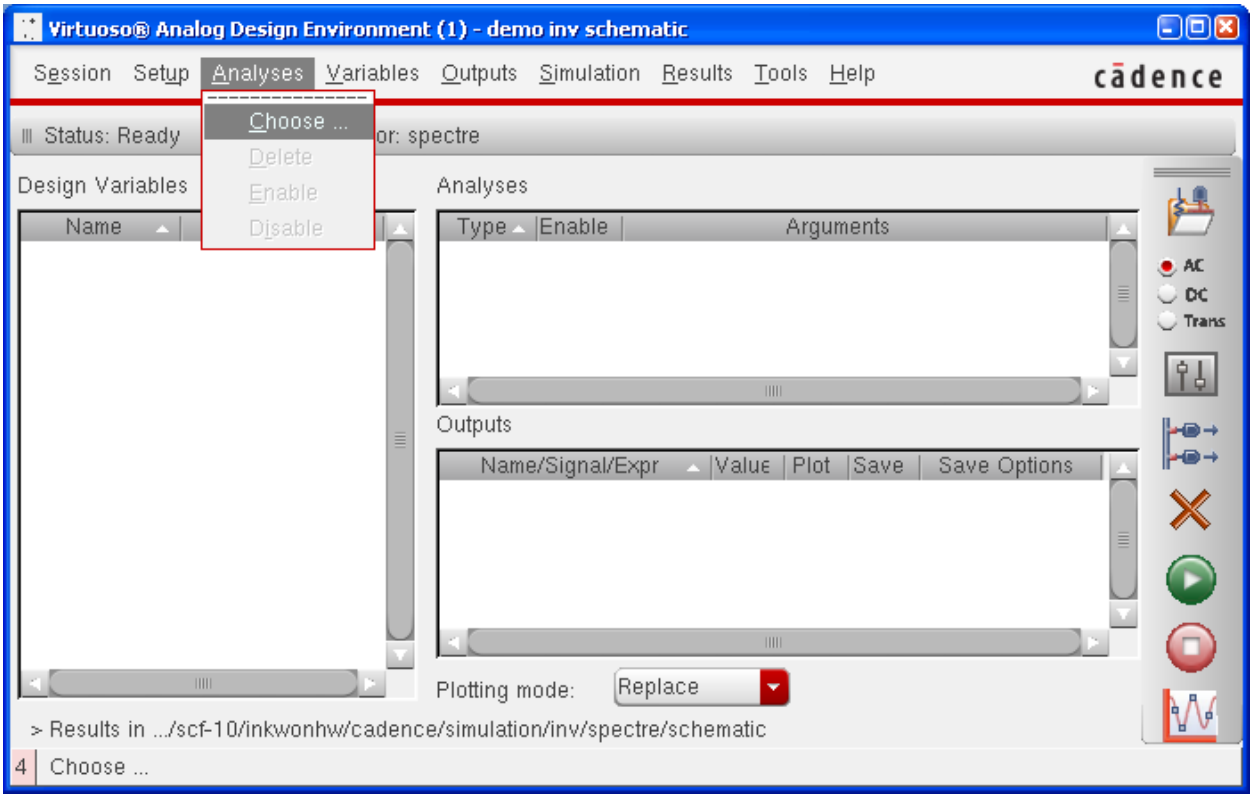
Input (change)



Remember to check Enabled button and then press OK or APPLY otherwise you will lose the configured numbers.

E. Choose a type of analysis - transient

You can choose „dc“ if you want to do dc analysis



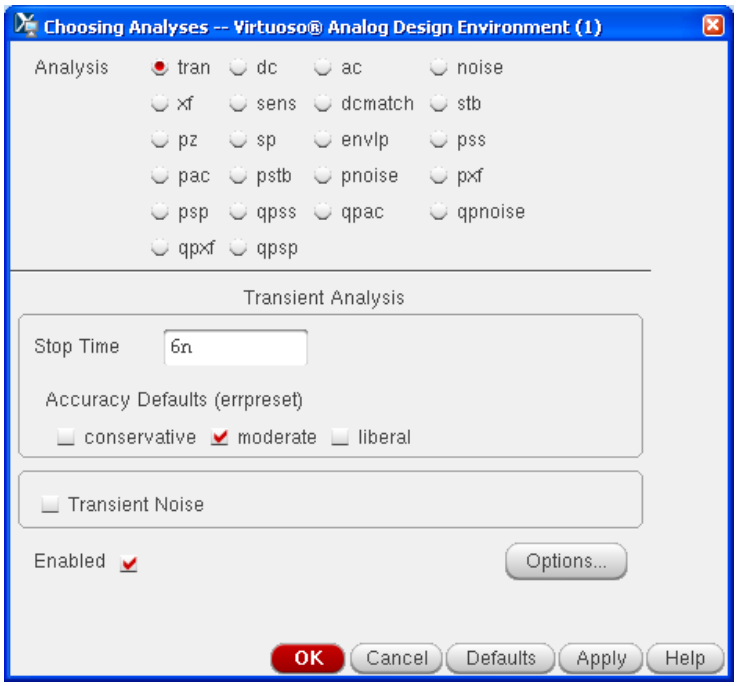
A. Choose tran

B. Give Stop time which means how long you want to simulate

C. Select moderate as accuracy defaults

D. Do not check Transient Noise

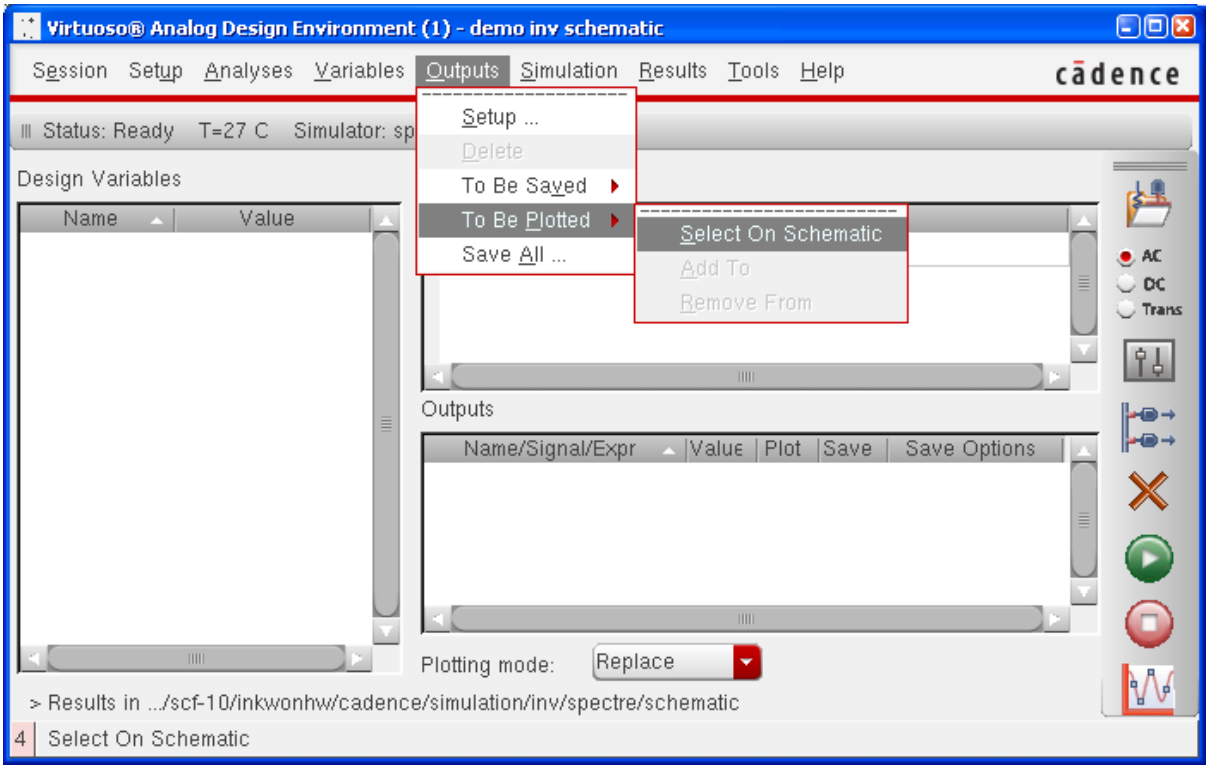
E. Check Enabled



F. Select signals to plot

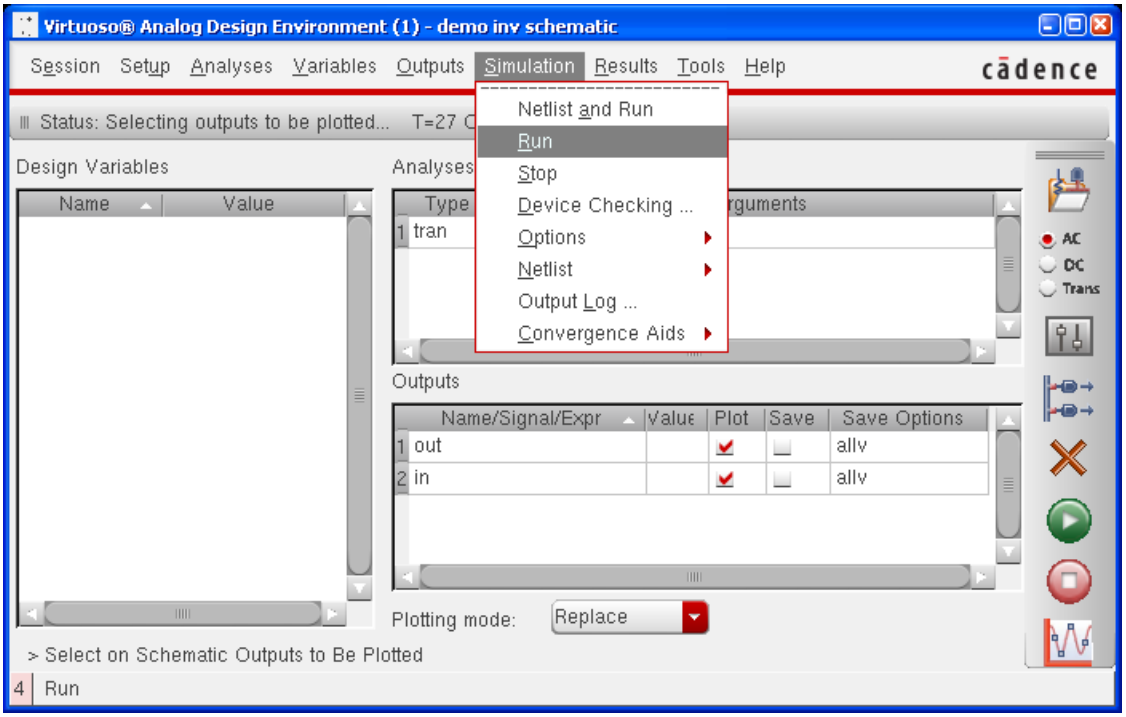
Outputs → To Be Plotted → Select On Schematic

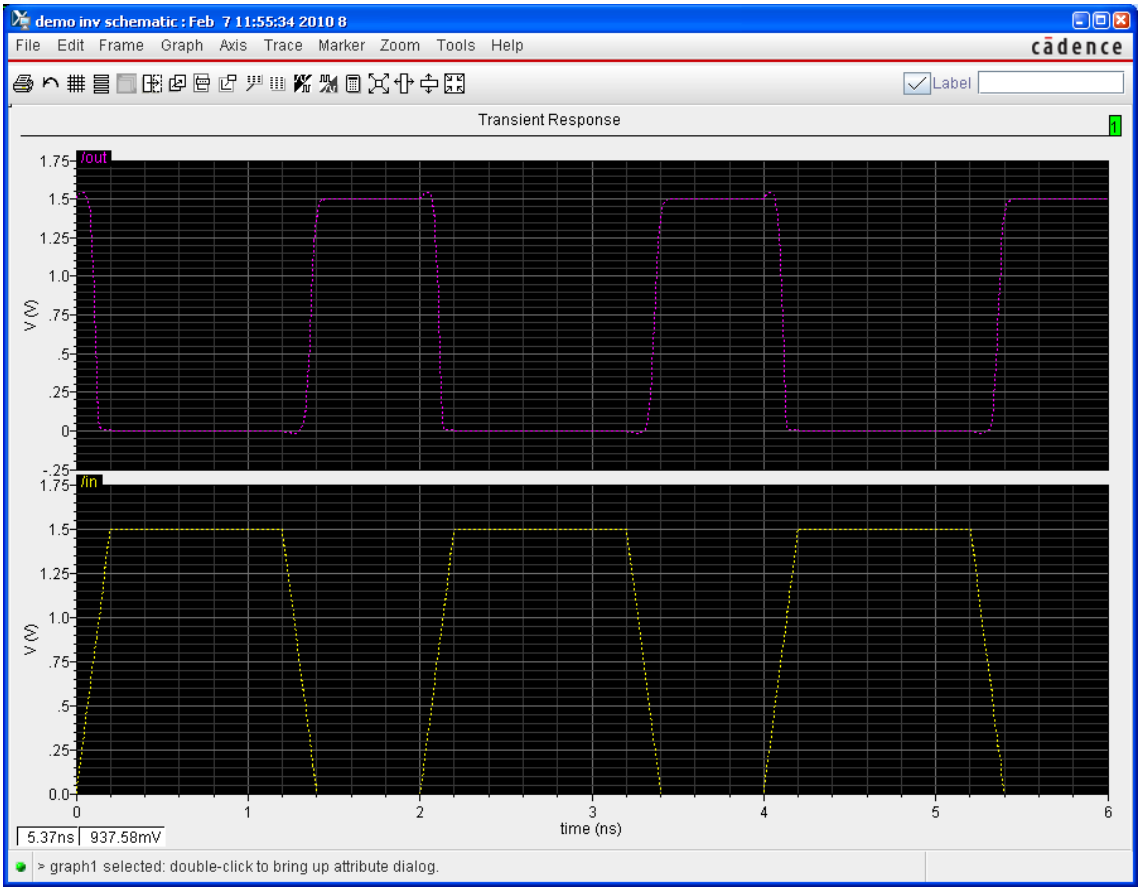
Click a signal (Pin) on a schematic/extracted. In Extracted try to use pins for signal that you need in the simulation because it is hard to select a net in the extracted view.



G. Run simulation

Simulation → Run



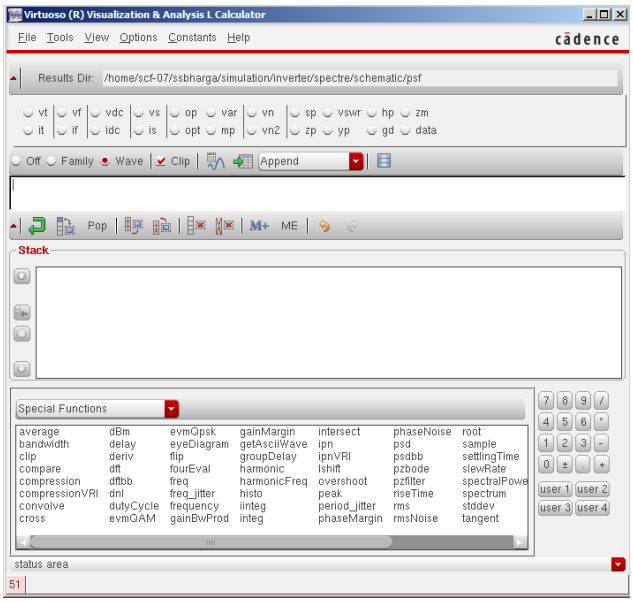


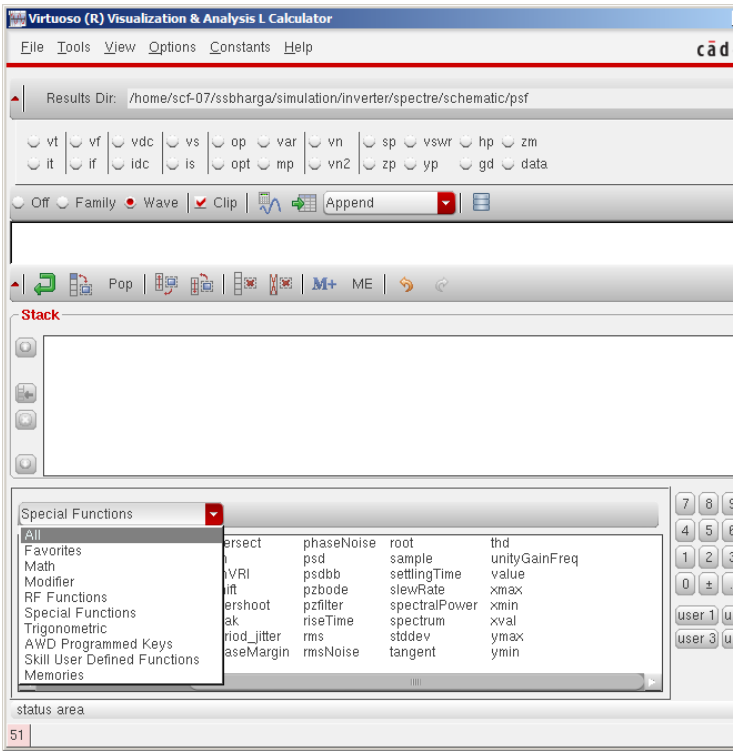
If you see a waveform like above picture, you followed every step properly.
Good job!.

H. Measurement

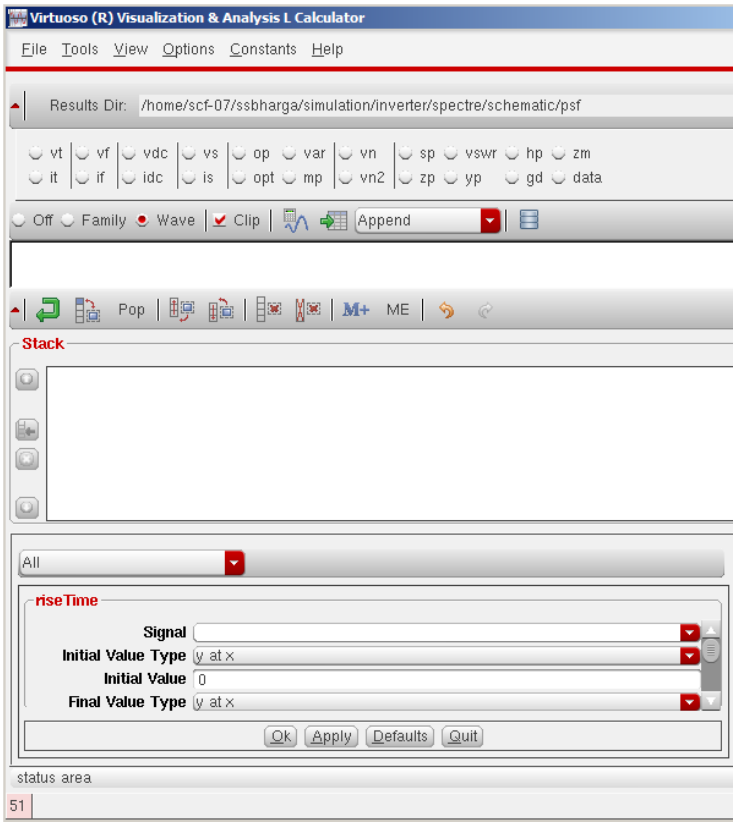
The following steps describe the measurement of rise time. Using similar steps other parameters of delay, fall time can be estimated.

Invoke the calculator  or tools-> calculator , select the Wave radio button:

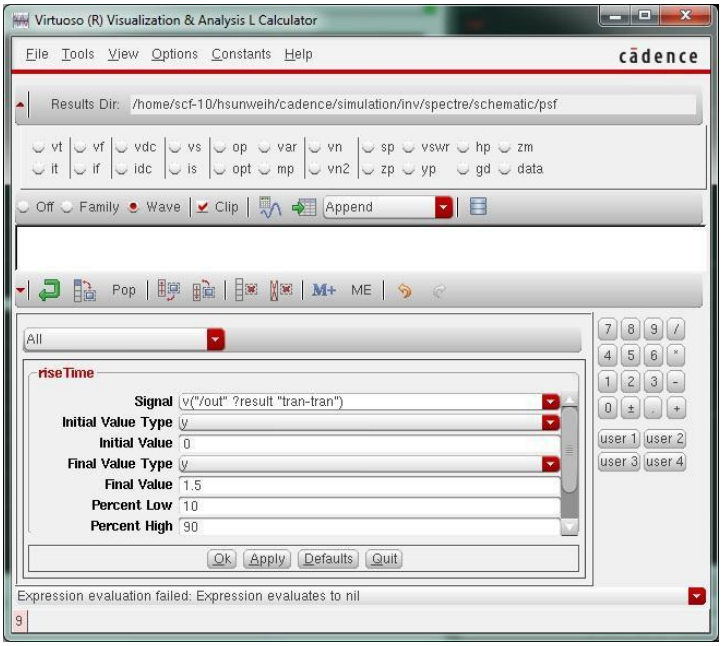




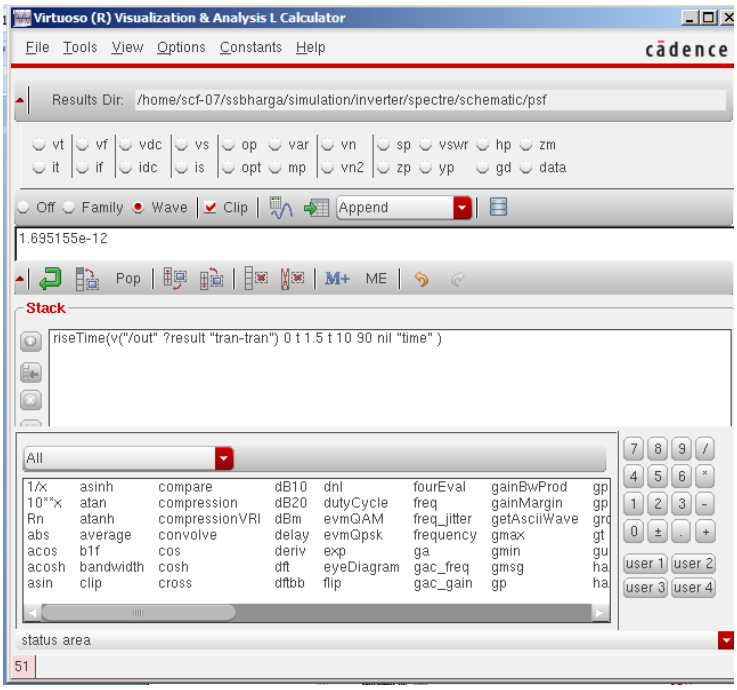
In the functions window – choose "all"



Select the rise time option



Select the signal from the waveform window whose rise time needs to be determined and click “OK”:



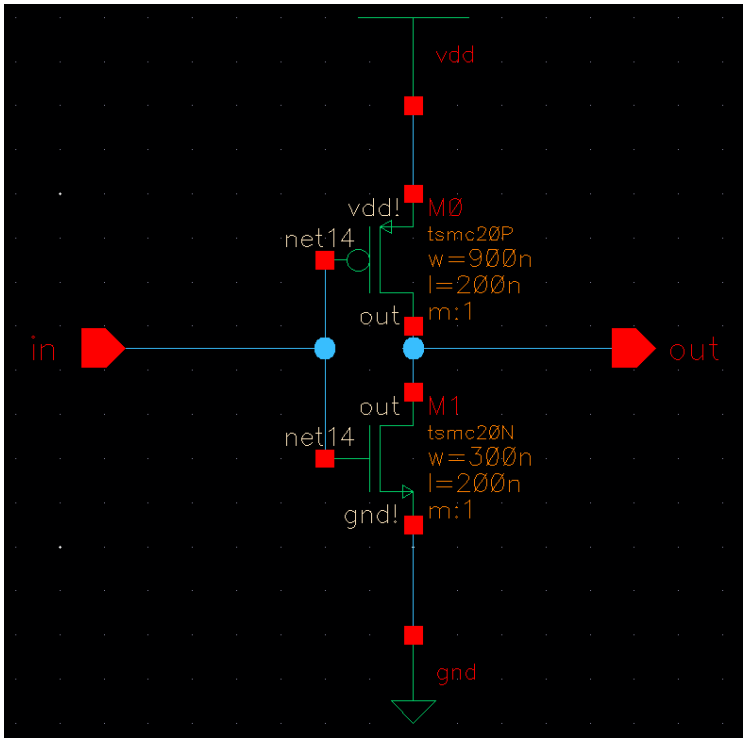
Click the evaluate buffer →  to display results as follows

You can also select a signal from calculator for example cos(Vin) as one of the plotted signals and you can see the results whenever you run the simulation.

Remember to save the simulation setup to use it later. You can do so by clicking on **Session → Save State** in the ADE (Analog Design Environment) window. Next time you want to simulate the same cell, you can reload your configuration by clicking on **Session → Load State**.

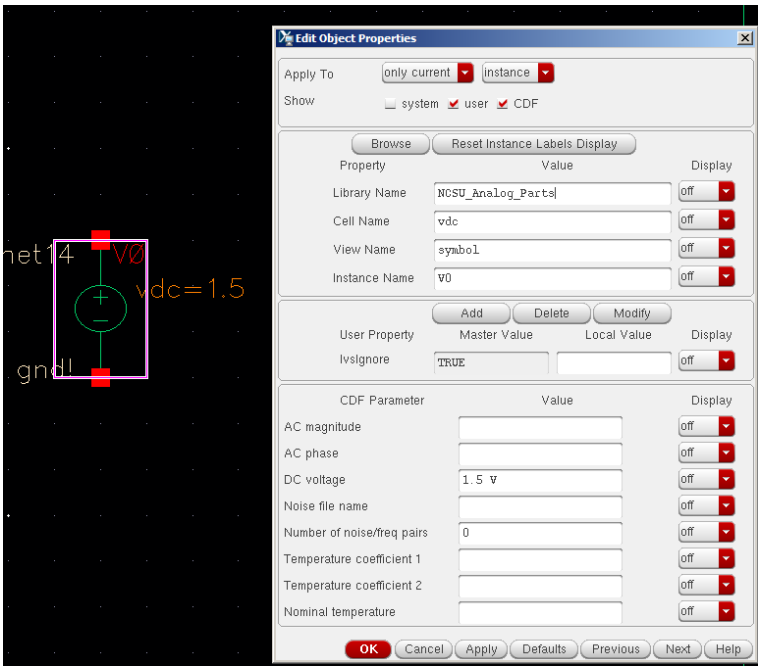
5. Run Spectre simulation (DC analysis)

The following inverter schematic is already created



A. Voltage Source

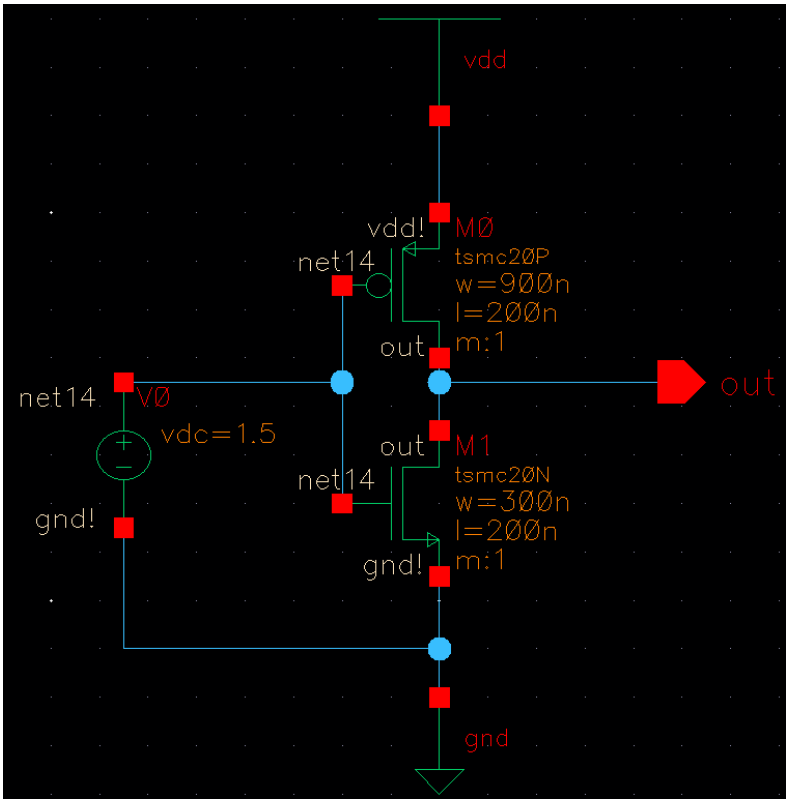
For DC analysis , the input pin “in” must be altered. The following are the steps to alter the pin “in” : Create→instance→NCSU analog parts→Voltage_sources select Vdc



The DC voltage must be set to 1.5V as shown.

B. Replace Input Pin

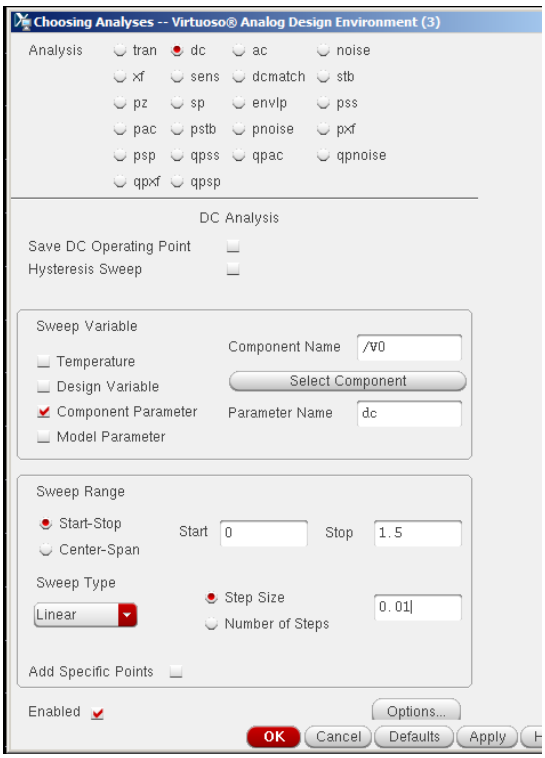
The Input pin “in” must be replaced with the above voltage source as shown below



Check and Save (make sure you get no errors)

C. Choosing Analyses

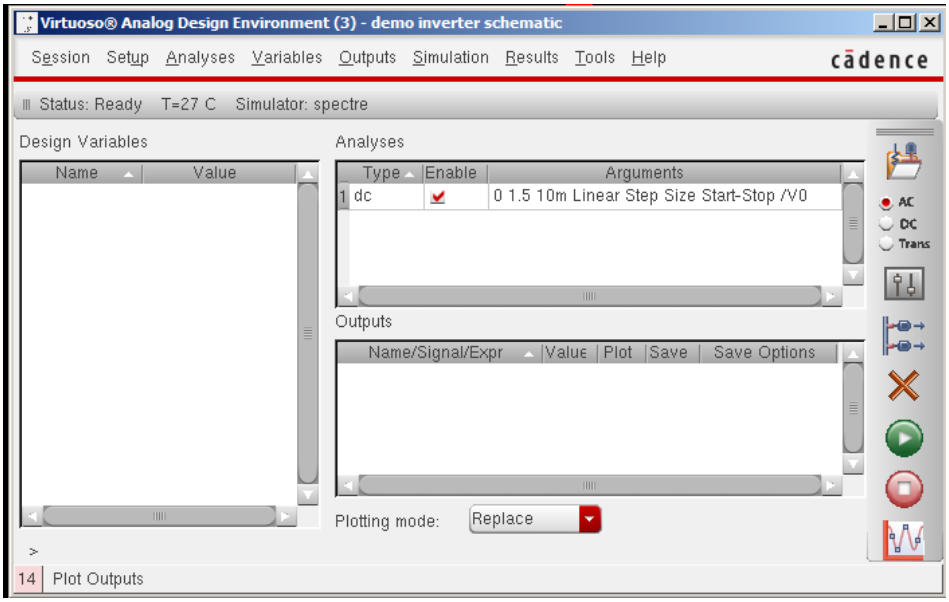
Launch ADE L, repeat steps A to D in section 3 of „Basic Design Flow“ except that there is no “in” input signal this time.



Go to Analyses → Choose dc

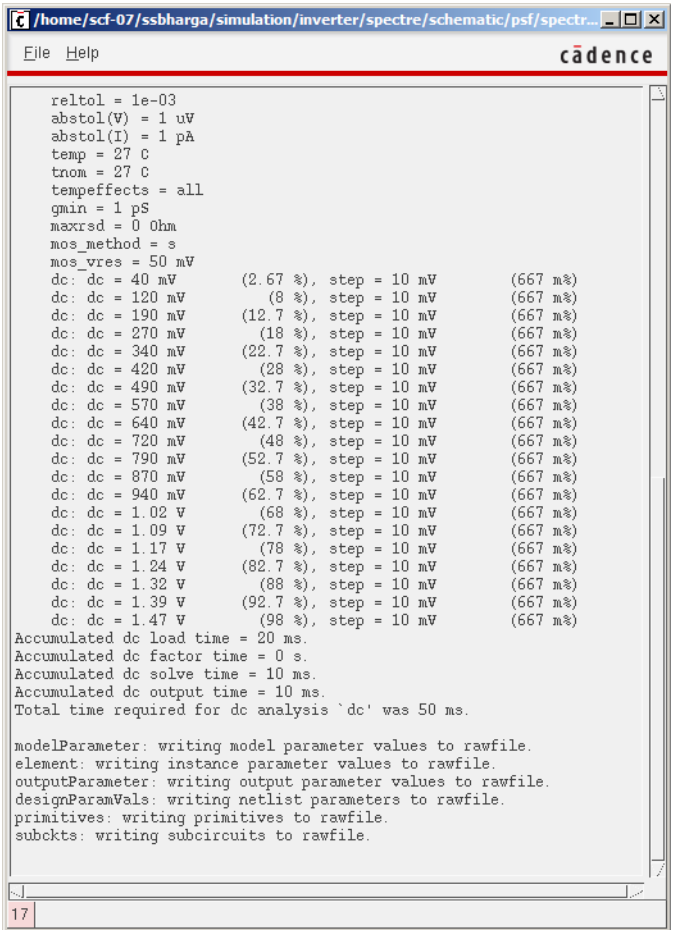
Choose „Component Parameter“,
Select Component, then the voltage source in the schematic, then choose 0 as Start, 1.5 as Stop and 0.01 as step .

Make sure that there are no other analyses selected apart from DC

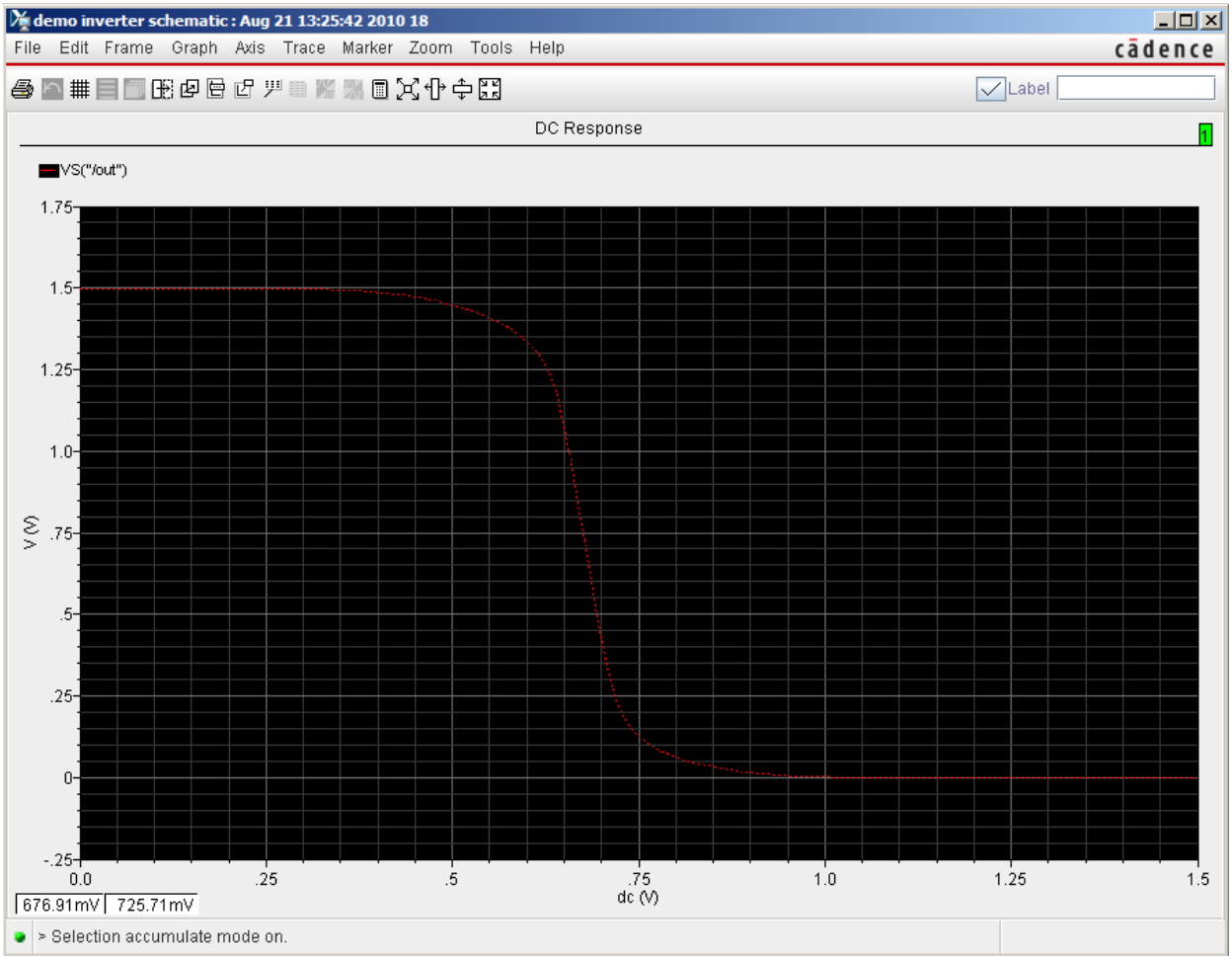


D. Run Simulation

Do simulations→netlist and run. On successful completion we get the following



Now, go to the results→Direct plot→DC. Click on the output pin “out” on the schematic and ESC key to get the following VTC

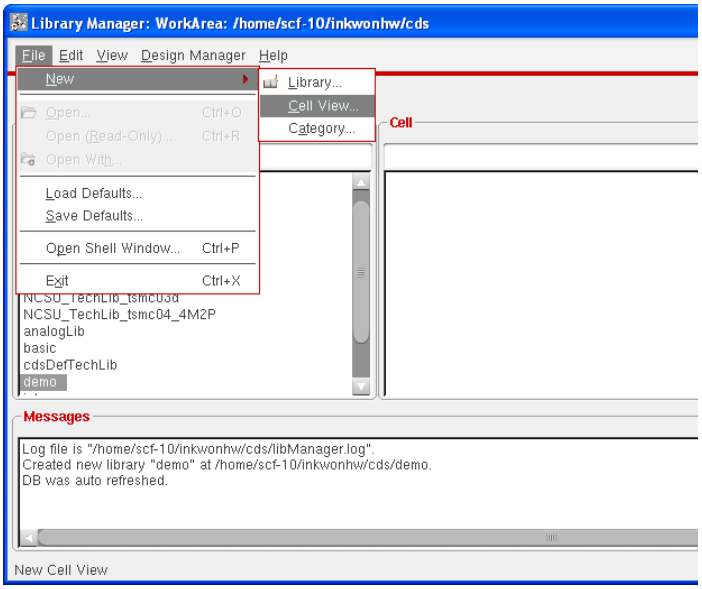


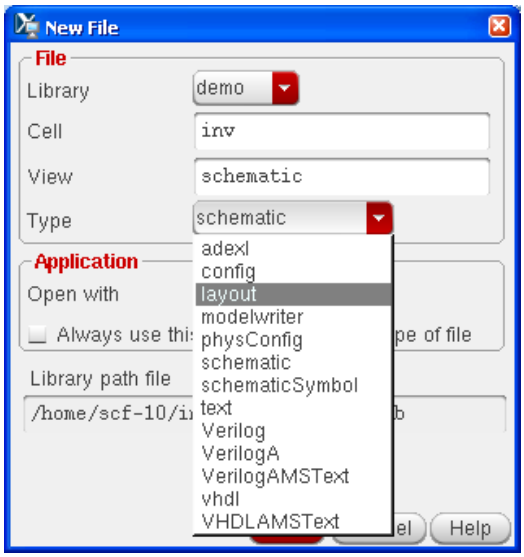
6. Layout

It‟s time to draw layout. Schematics are for verifying your design very roughly. They don‟t consider physical features like parasitic capacitances. After determining your design variables by schematics, you need to draw layouts.

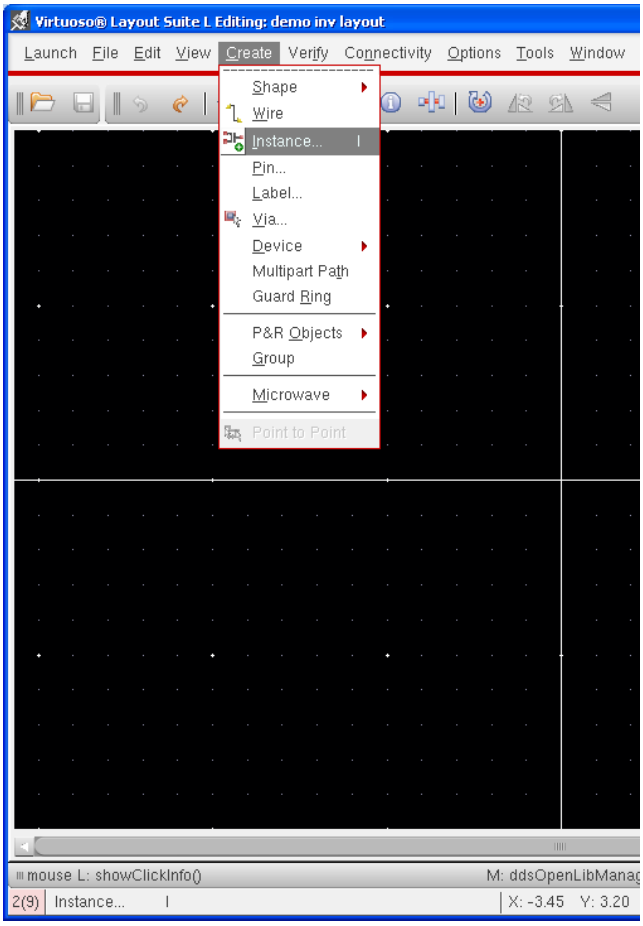
Design flow of layouts is very similar to one of schematics, but it has additional step which is LVS check. It is for check if your layout is identical to the schematic or not. Hence, this step is very important. If your logic doesn‟t pass this step, you may lose significant points for that.

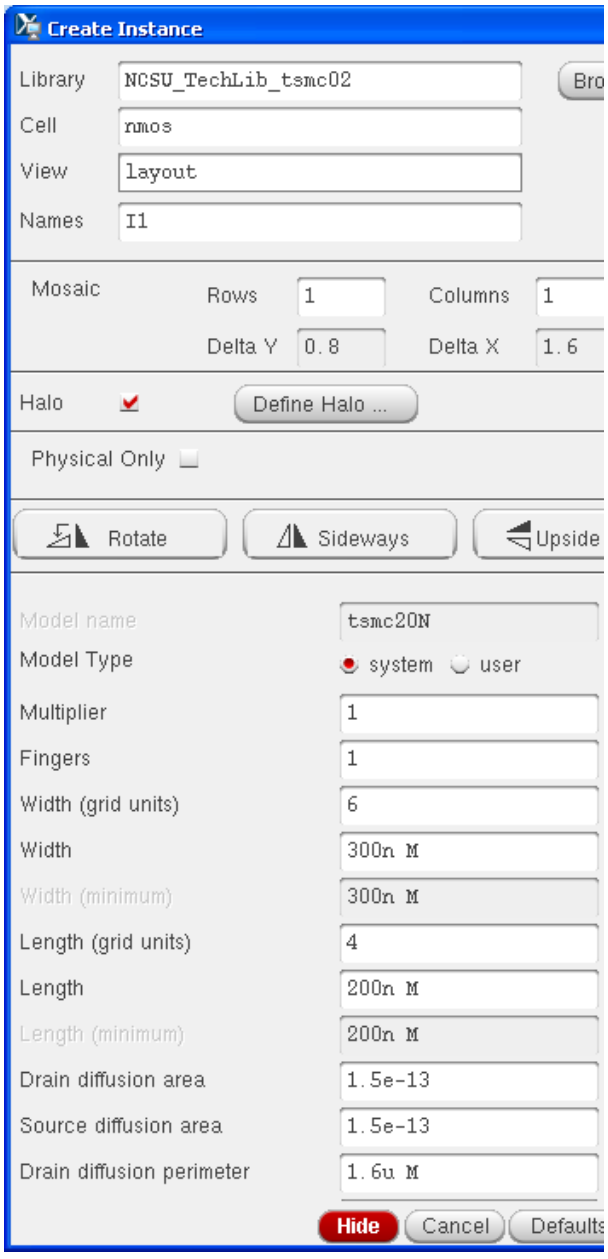
A. Create a layout

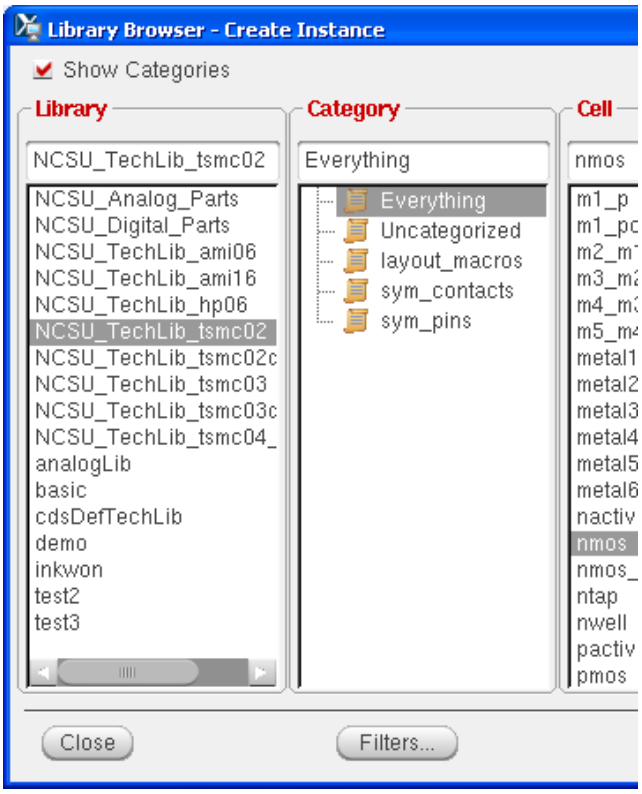




B. Add an instance - nmos

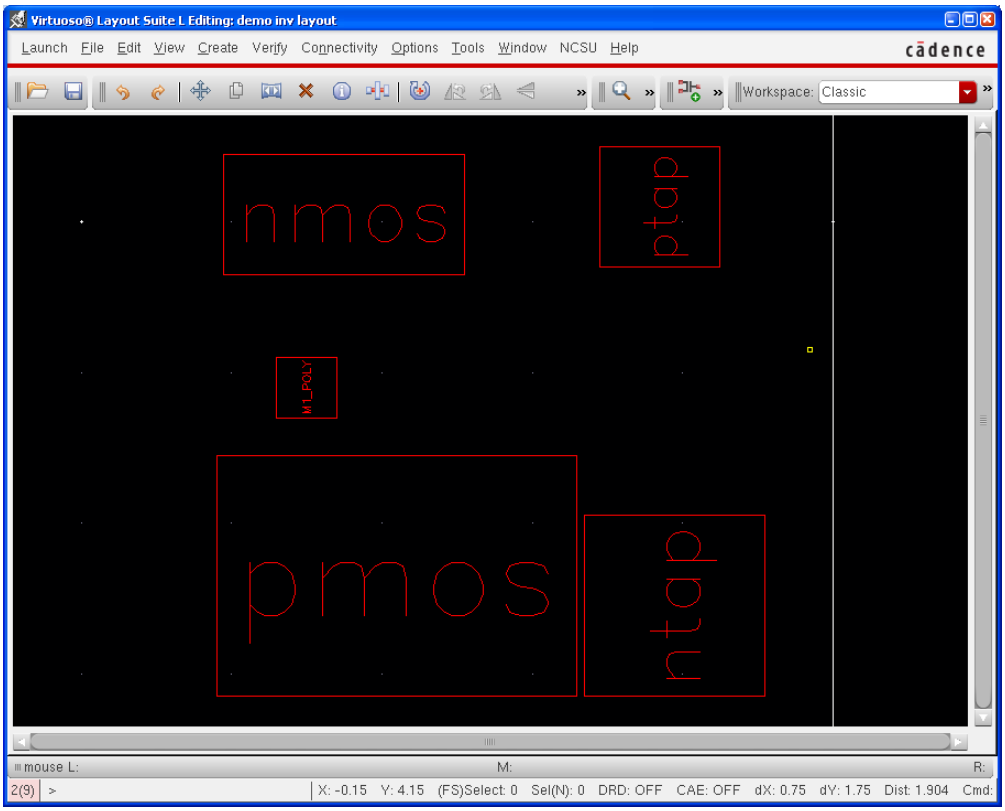




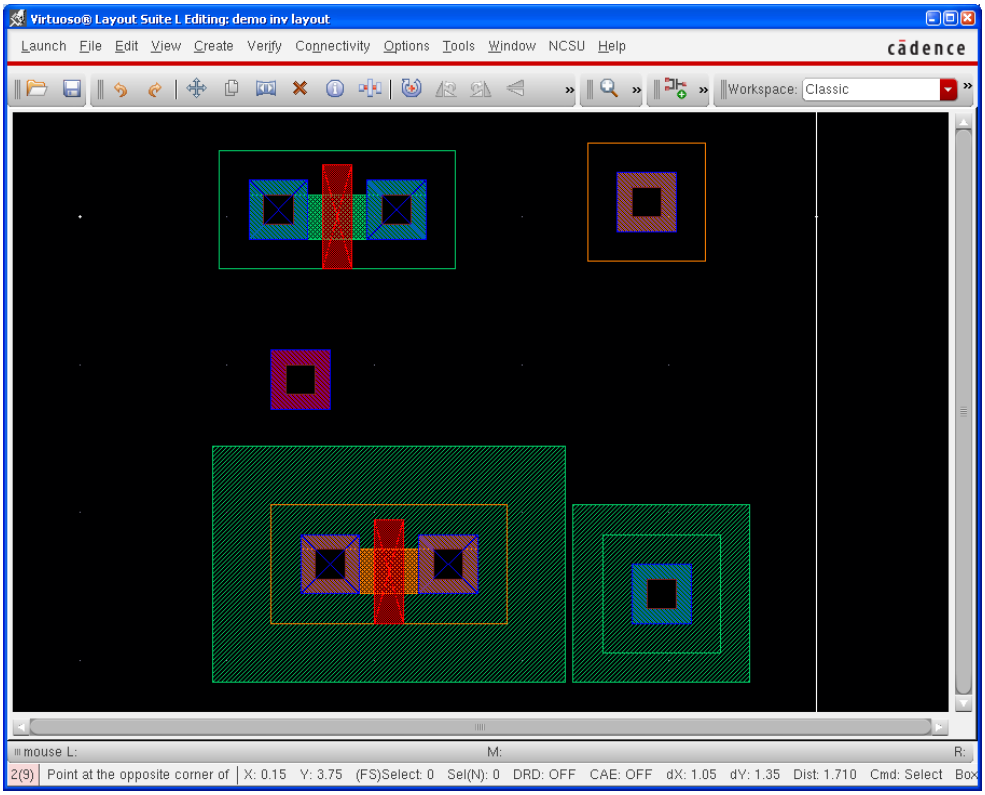


You can modify width of transistors.

C. Add more instances – pmos, ptap, ntap, and m1_ploy



You can select alternate view of a layout. Try „Shift + f“ and „Ctrl + f“.

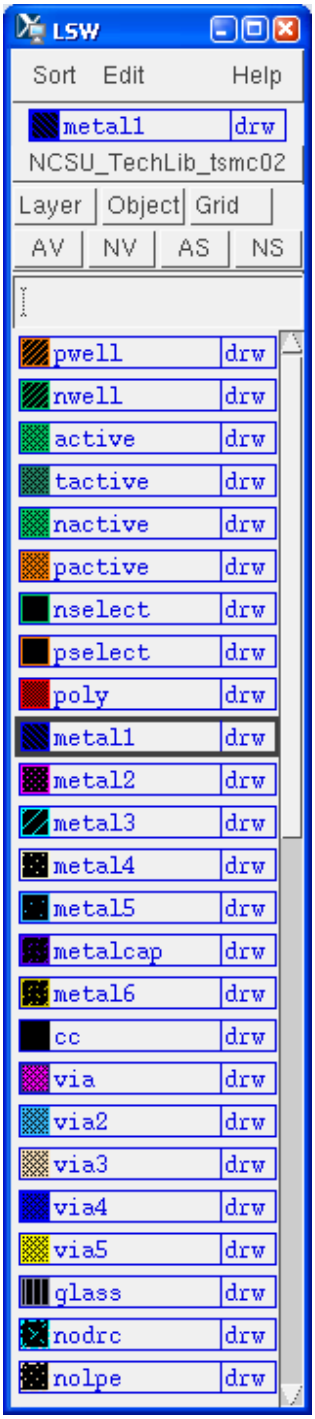


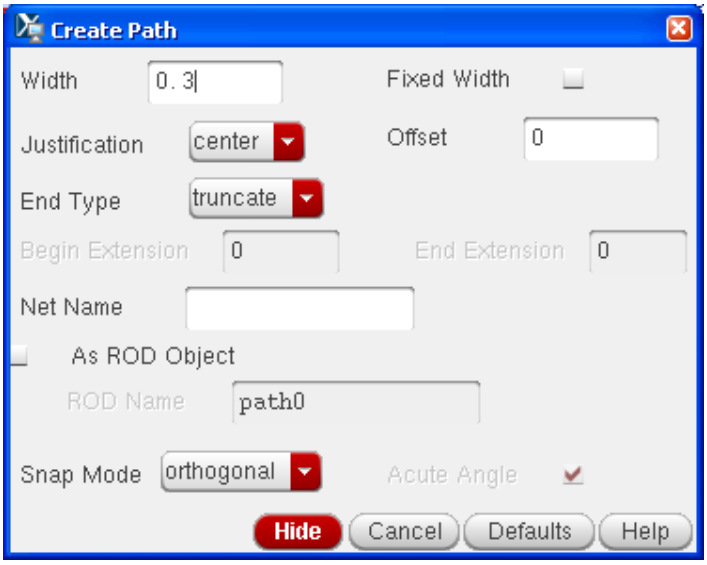
D. Draw metal1

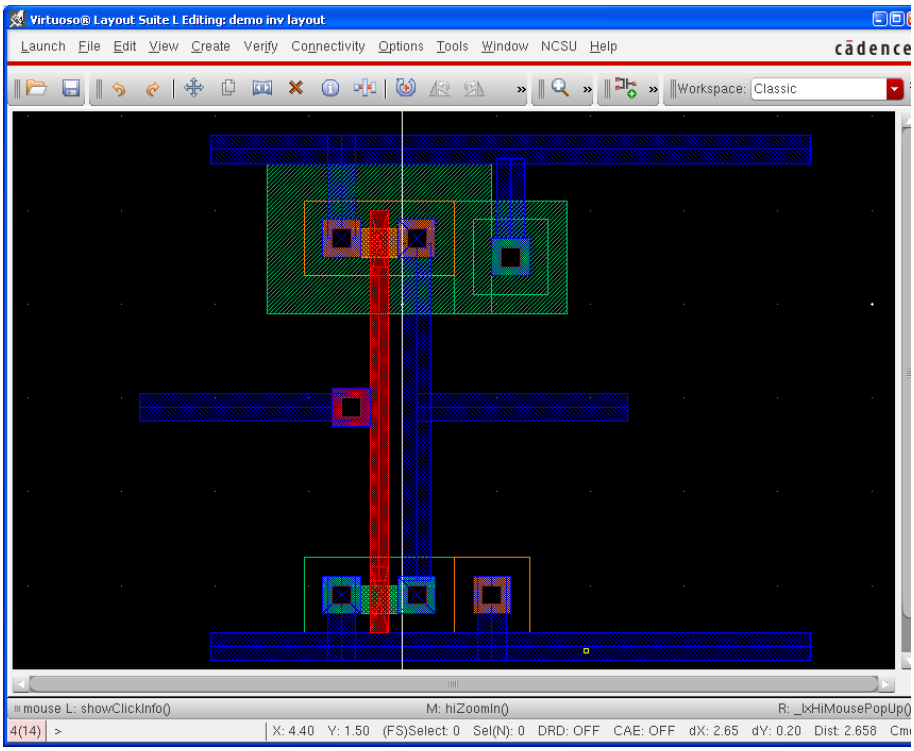
There are few ways for drawing metal, but I recommend you use „path“. It“s quite convenience than others.

Create → Shape → Path

First of all, you should select metal1 on LSW window. Default width for metal1 is 0.3, which means 300nm (3 λ). You can draw metal layer simply by clicking



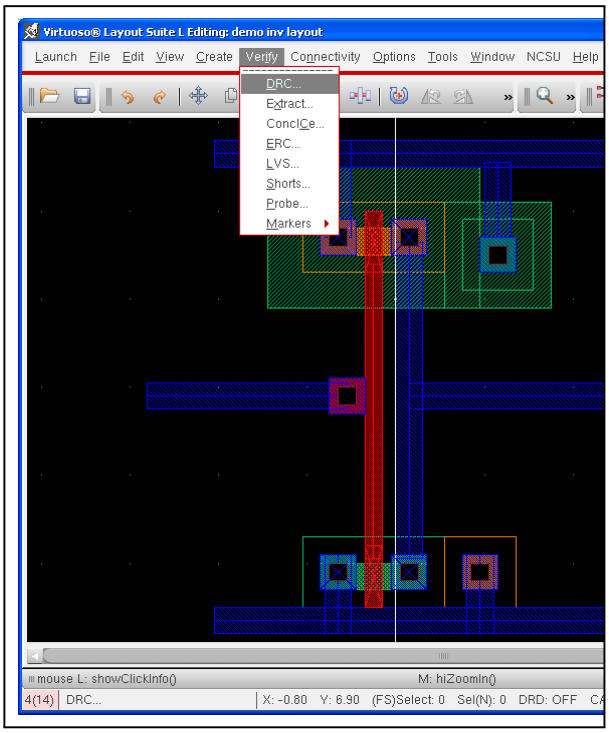


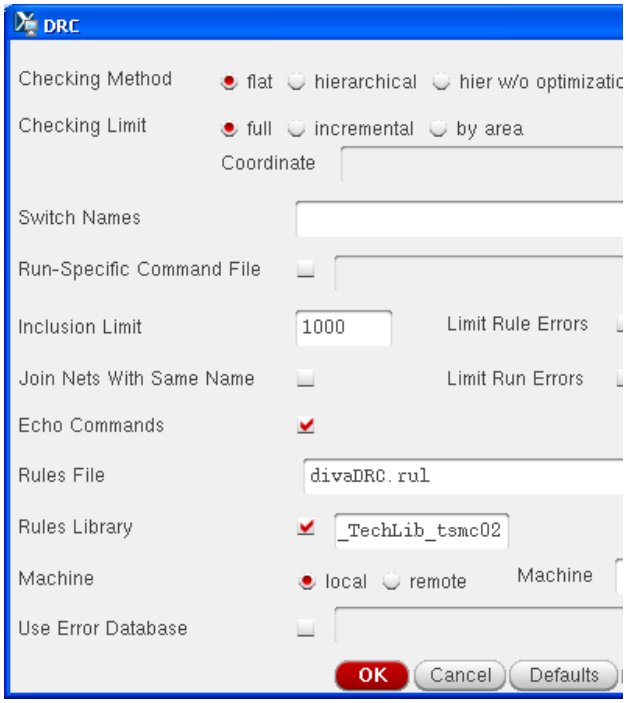


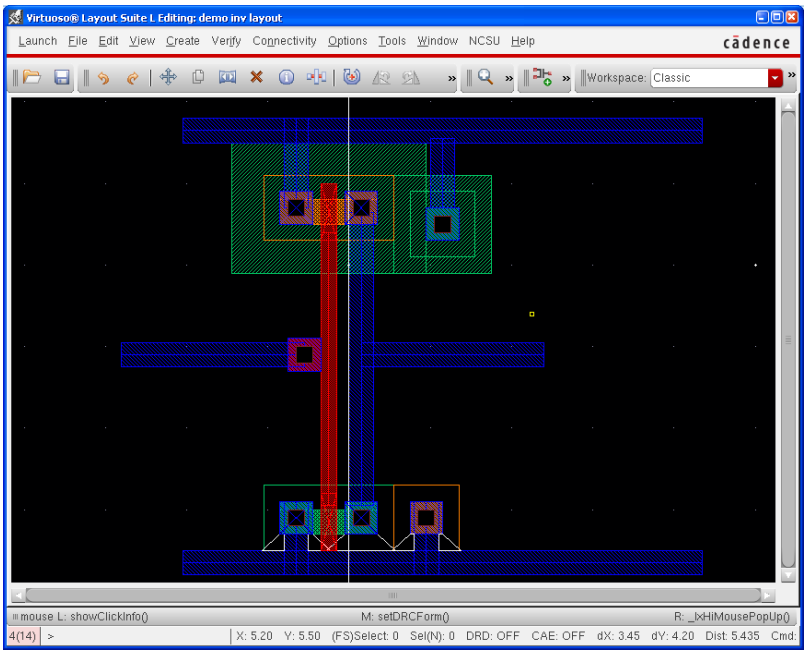
E. Run DRC

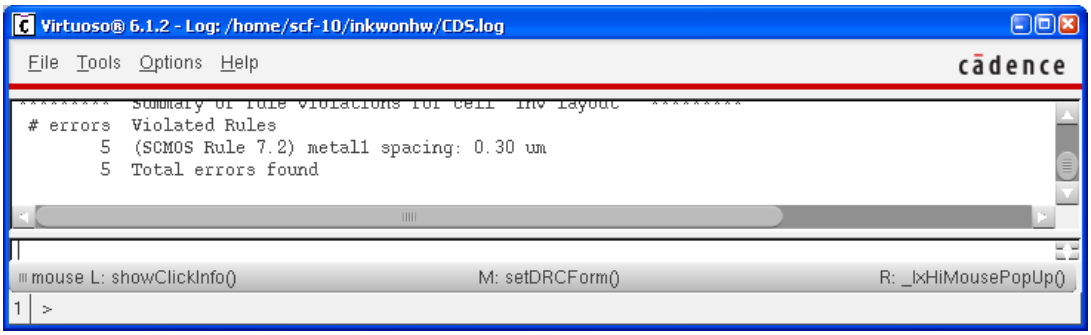
This step checks if your layout follows design rules.

Verify → DRC

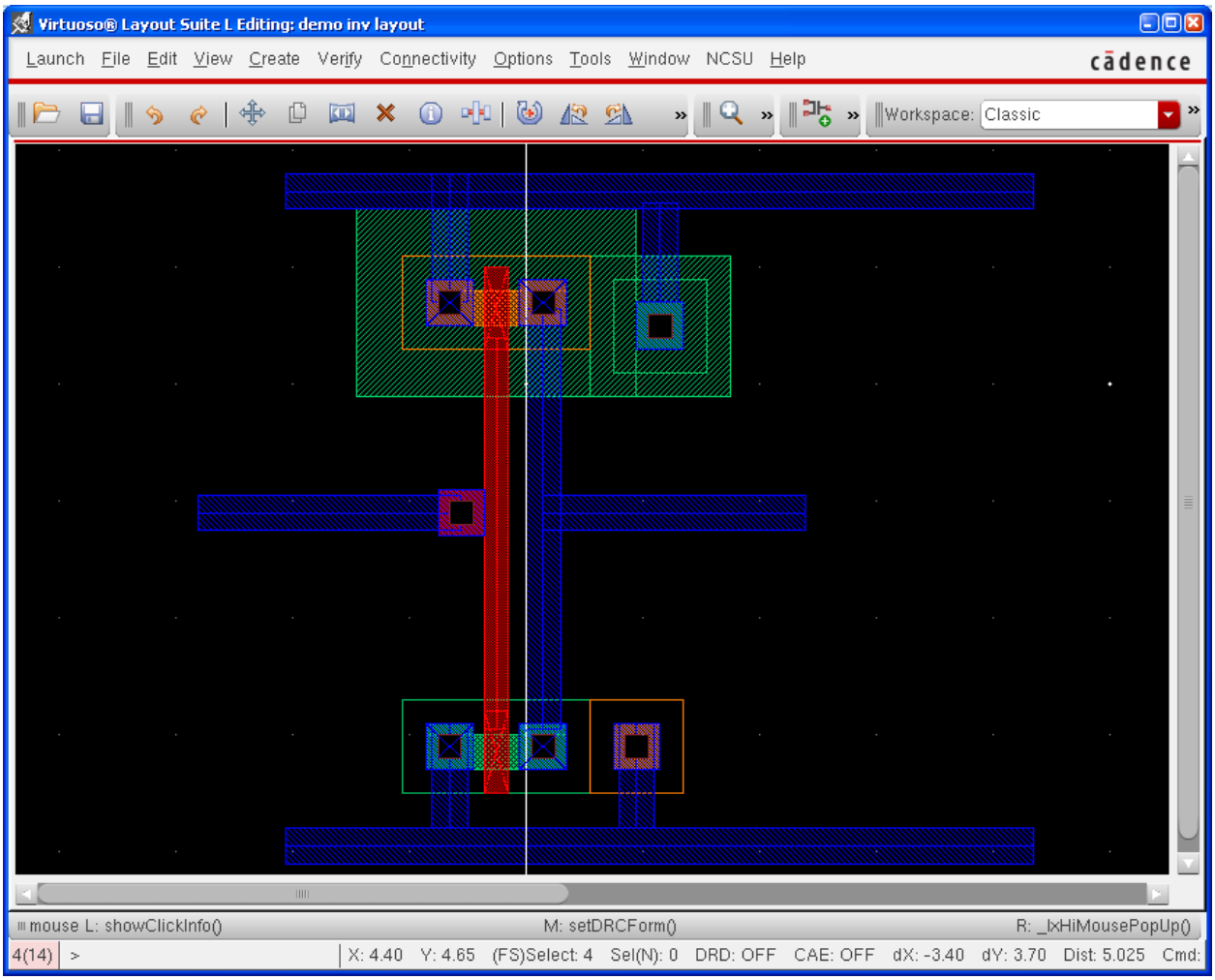


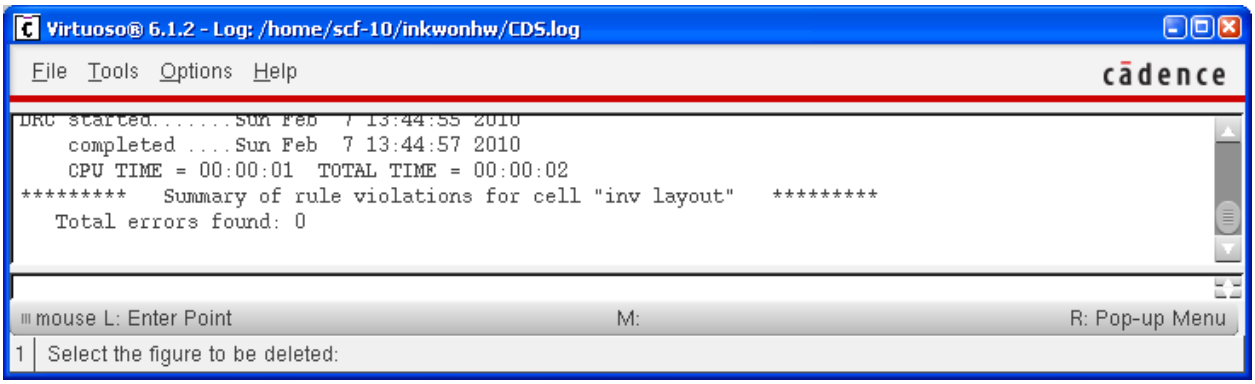






We have five errors. It is because a gnd metal layer is too close to an nmos transistor.
After modifying layout, run DRC again.



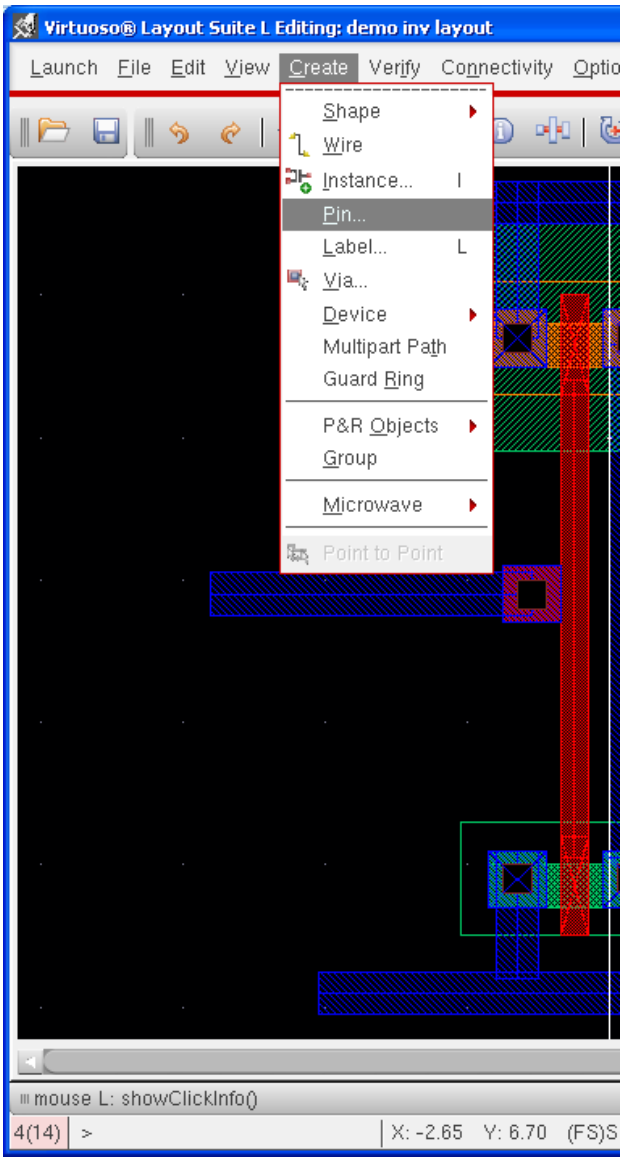


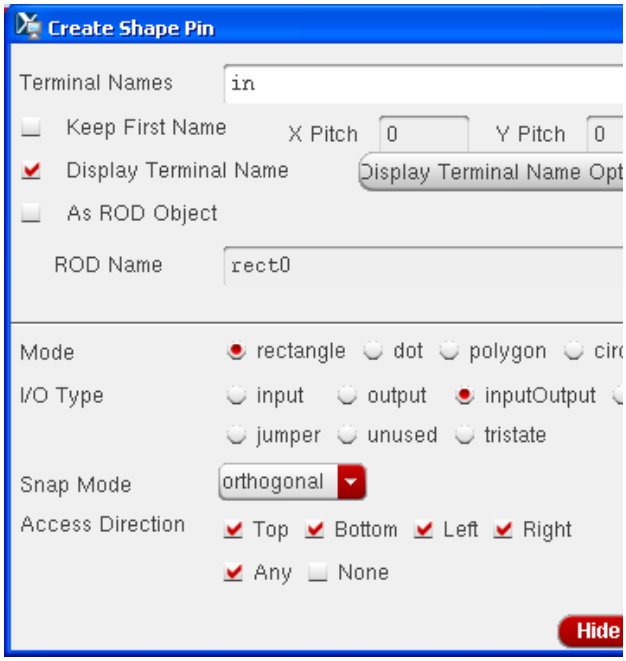
There is no error!!

F. Add pins

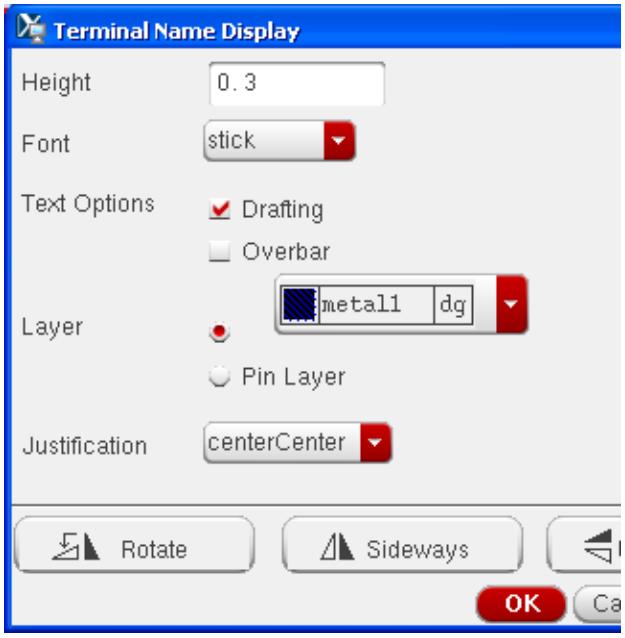
We had two pins on a schematic, which are „in“ and „out“. Pins are for assigning signals to physical device, so we assign voltage level of gnd and vdd by using pins. Hence, we have 4 pins for the layout, which are „in“, „out“, „gnd!“, and „vdd!“.

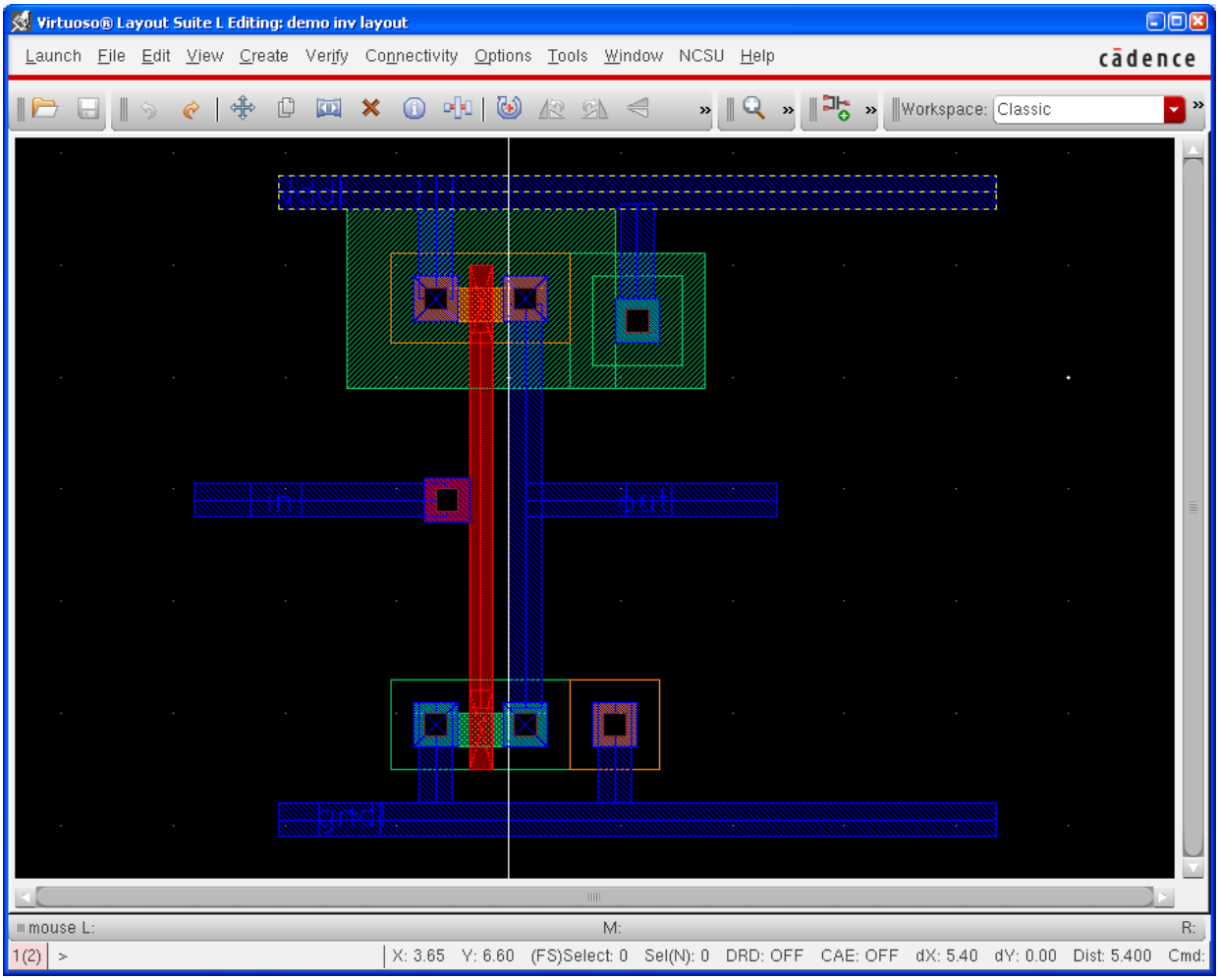
Create → Pin





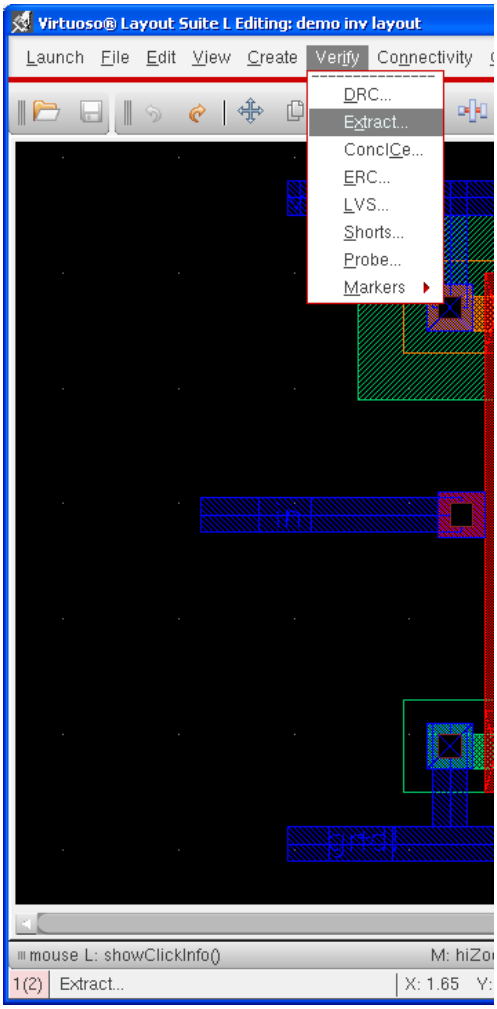
Check „Display Terminal Name“ if you want to see pin name on the layout.
Click „Display Terminal Option

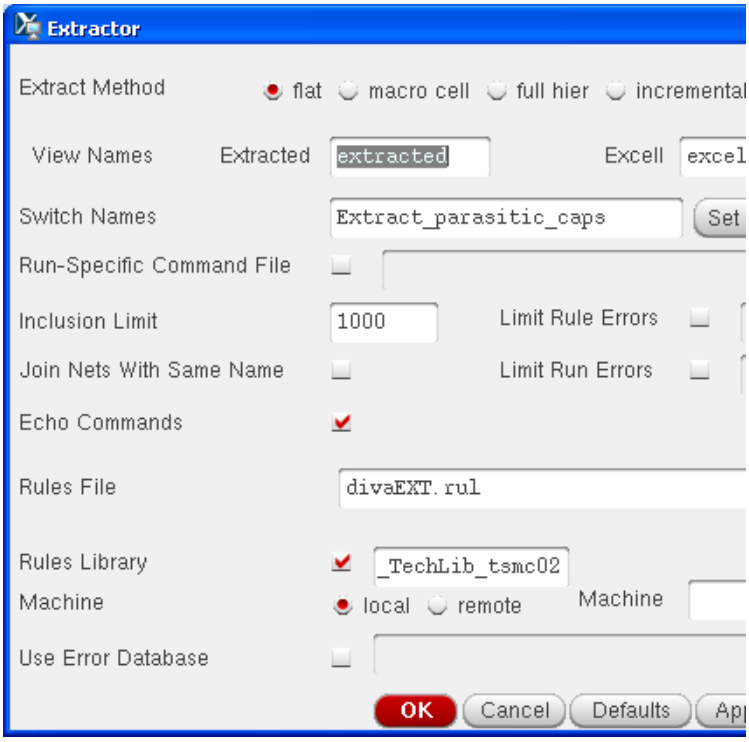



Virtuoso® Layout Suite L Editing: demo inv layout
Launch File Edit View Create Verify Connectivity Options Tools Window NCSU Help
cadence
Workspace: Classic
mouse L:
M:
R:
1(2)
X: 3.65 Y: 6.60 (FS)Select: 0 Sel(N): 0 DRD: OFF CAE: OFF dX: 5.40 dY: 0.00 Dist: 5.400 Cmd:

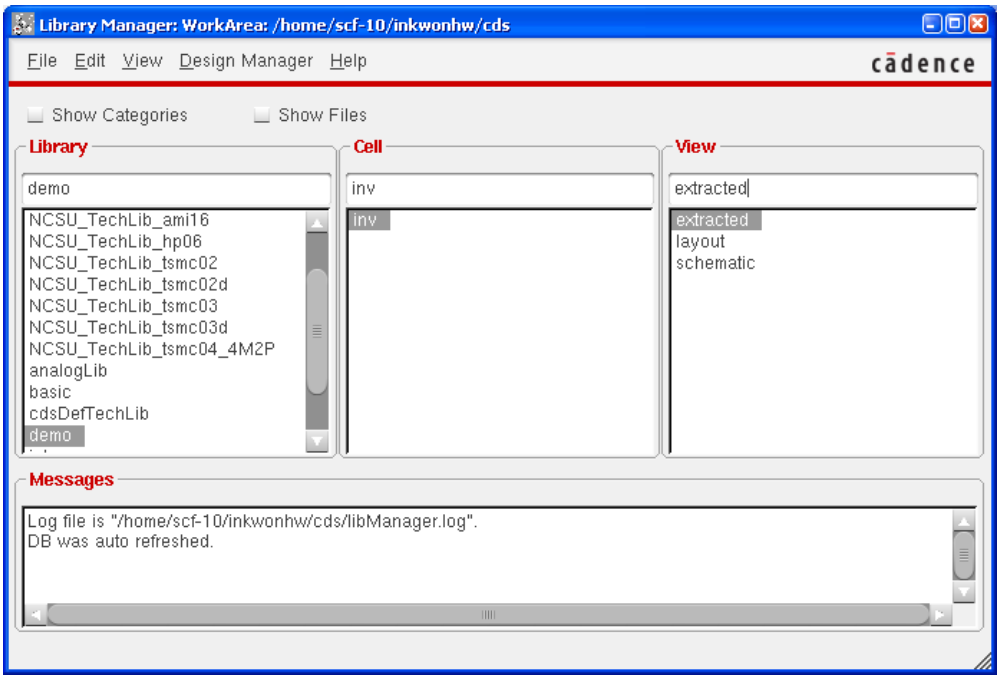
G. Extract

A layout is just a picture. If you need to run simulation using the layout, you should convert it to the other format. It is done by extracting. It‟s something like compiling a code.





Select „Extract_parastic_cap‟ as a switch name, otherwise your extracted design won‟t have parasitic capacitances.

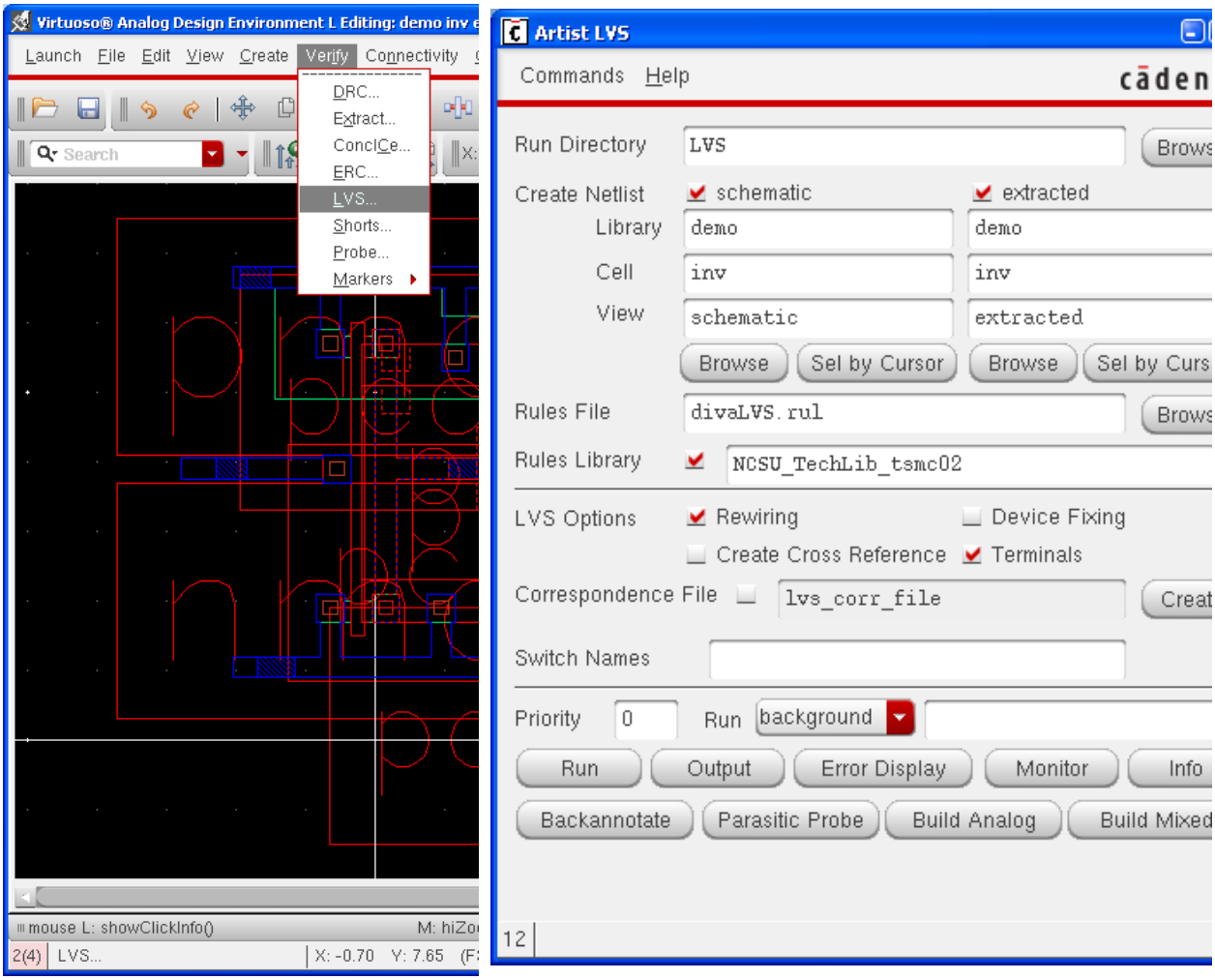


H. Run LVS

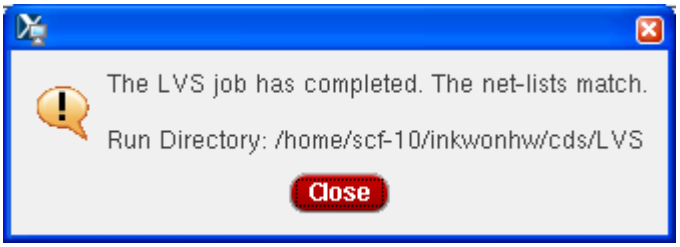
As I mentioned before, this step is very important for your grading. More complicated design, more time will be required for debugging LVS.

Verify → LVS

Keep in mind. You **SHOULD** compare your schematic with **EXTRACTED**.



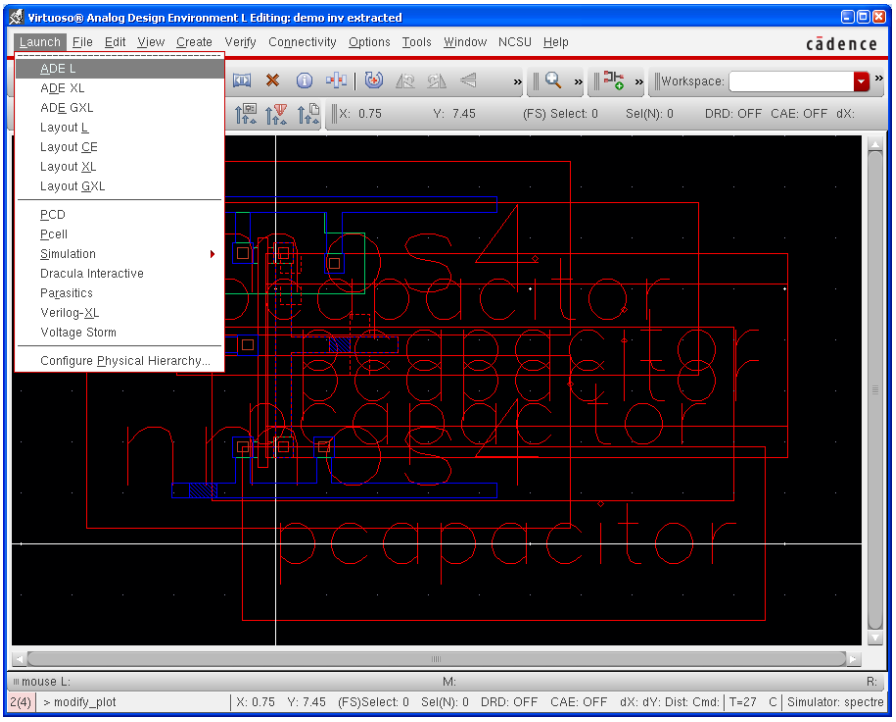
I hope all of you will see the following window.

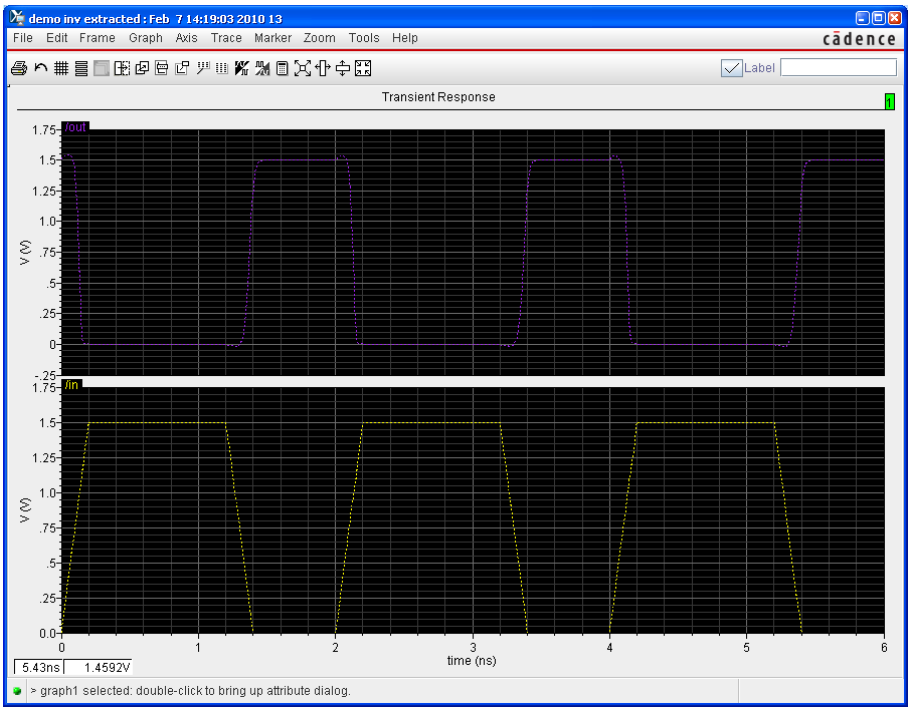


If there are errors, you can check the results by clicking „Output" button. „Error Display" also might be helpful.

I. Run Spectre simulation

It is same as schematics. Please follow the instructions for the schematics.





Congratulations!!

You followed all steps I prepared. Let‟s do the same thing for more complicated designs.

*Some useful information

Useful Links:

http://www.edaboard.com/

http://www.eda.ncsu.edu/wiki/NCSU_EDA_Wiki

http://www.cadence.com/community/forums/