Spiral 2-6

Semiconductor Material
MOS Theory

Learning Outcomes

- I understand why a diode conducts current under forward bias but does not under reverse bias
- I understand the three modes of operation of a MOS transistor and the conditions associated with each mode
- I can analyze circuits containing MOS transistors to find current and voltage values by first determining the mode of operation and then applying the appropriate equations

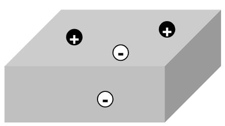
Current, Voltage, & Resistors

- Kirchoff's Current Law
  - Sum of current _______ a node is equal to current coming _____________ a node
- Kirchoff's Voltage Law
  - Sum of voltages around a loop is _______
- Ohm's Law (only applies to resistors or devices that "act" like a resistor)
  - I = ____ or _____________________________
  - Note: For a resistor, current and voltage are _____________ related with R as the slope

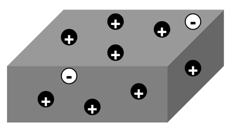
DIODES

Semiconductor Material

- Semiconductor material is not a great conductor material in its pure form
  - Small amount of free charge
- Can be implanted ("doped") with other elements (e.g. boron or arsenic) to be more conductive
  - Increases the amount of free charge

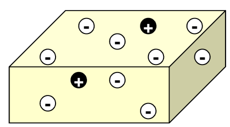


Pure Silicon



P-Type Silicon (Doped with boron)

Electron acceptors



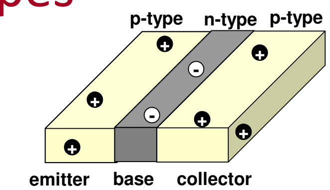
N-Type Silicon (Doped with arsenic)

Electron donors

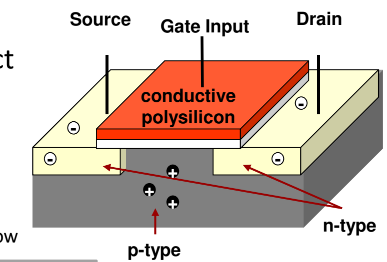
Transistor Types

- Bipolar Junction Transistors (BJT)
  - npn or pnp silicon structure
  - Small current into very thin base layer controls large currents between emitter and collector
  - However the fact that it requires a current into the base means it burns power (P = I*V) and thus limits how many we can integrate on a chip (i.e. density)
- Metal Oxide Semiconductor Field Effect Transistors
  - nMOS and pMOS MOSFETS
  - Voltage applied to insulated gate controls current between source and drain
    - Gate input requires no constant current…thus low power!

We will focus on MOSFET in this class



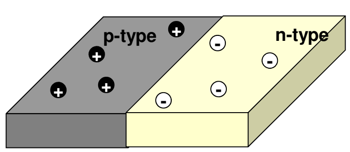
npn BJT



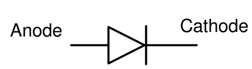
N-type MOSFET

PN Junction Diode

- Our understanding of how a transistor works will start by analyzing a simpler device: a diode
- A diode can be formed by simply butting up some p-type and n-type material together



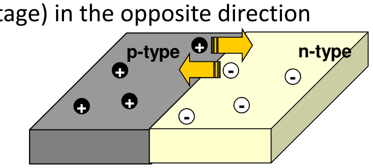
Physical view



Schematic symbol of a diode

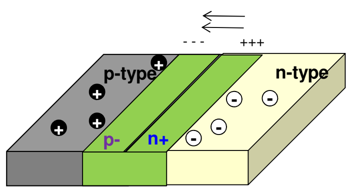
The PN Junction

- When we join the two substances the free electrons at the junction will combine with the nearby free holes in a "loose" bond
- This has two effects:
  - Around the junction there are ______________ free charges (they've all combined) creating a _______________________
  - Now remember the dopants in n- and p-type material are still _____________ charged (same # of protons/electrons). So this migration has actually created ions and thus an ________________ (and thus voltage) in the opposite direction



Depletion Region

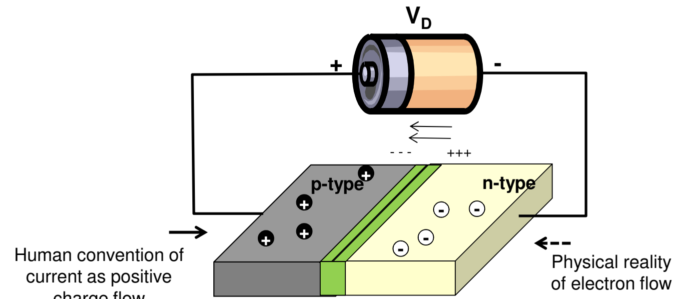
- Depletion region has __________ free or mobile charge
- A small ___________ is induced due to this recombination
  - N-type material LOST an electron leaving a _________ ion
  - P-Type material LOST a hole (GAINED an electron) leaving a ___________ ion
  - The voltage is in the opposite direction



Depletion Region

Forward Bias

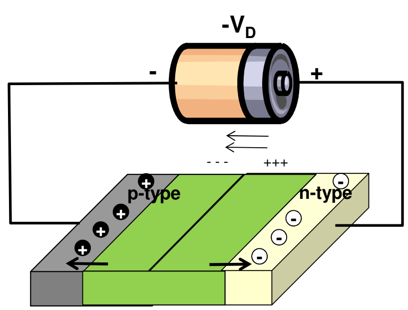
- Now let's place an external positive voltage source across the diode
  - Holes and electrons are pushed toward each other and reduce the depletion region
  - If the external voltage is high enough the charges will have enough ________ to overcome the gap and start ______________ through the diode
  - The positive external voltage needed to overcome the depletion region is known as the _________________ Voltage



Depletion Region

Reverse Bias

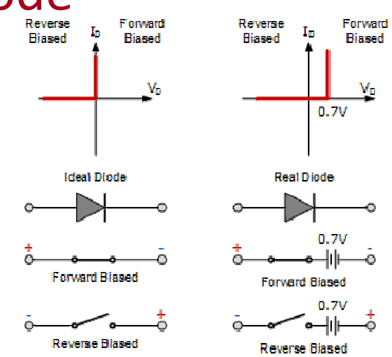
- Now let's place an external negative voltage source across the diode
  - Holes and electrons are attracted to the voltage source terminal (pulled away from the depletion area making the depletion area expand)
  - ______ current is flowing across the junction because both holes and electrons are attracted in opposite directions

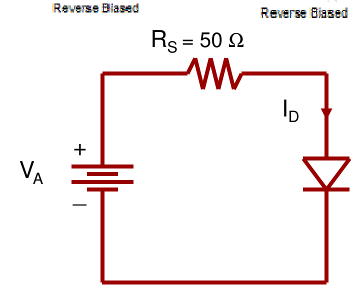


Depletion Region

Ideal Diode

- A perfect diode would ideally allow current to flow in ____________________
- It would therefore be a perfect conductor in one direction (forward bias) and a perfect insulator in the other direction (reverse bias)
- Example: Determine the value of ID if a) VA = 5 volts (forward bias) and b) VD = -5 volts (reverse bias)
  - Ideal model:
    - a) I_D = _______ = __________ = 100 mA
    - b) Diode is in reverse bias and is acting like a perfect insulator, therefore no current can flow and I_D = ______
  - More realistic:
    - a) I_D = ____________/R_S = 86 mA
    - b) I_D = 0

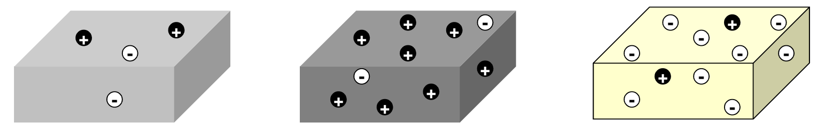




TRANSISTORS

Carrier Concentration

- Even silicon has some amount of free electrons (n) and holes (p)
  - We refer to this as the ______________________ concentration
  - Note: n = p since a free electron leaves a hole behind
- When we add dopants we change the carrier concentration
  - N_A and N_D is the concentration of __________ and ___________ respectively
  - Note: $N_A >> p$ and $N_D >> n$



Pure Silicon

P-Type Silicon (Doped with boron)

Electron acceptors

N-Type Silicon (Doped with arsenic)

Electron donors

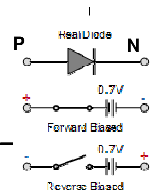
Doped Valence and Conduction Bands

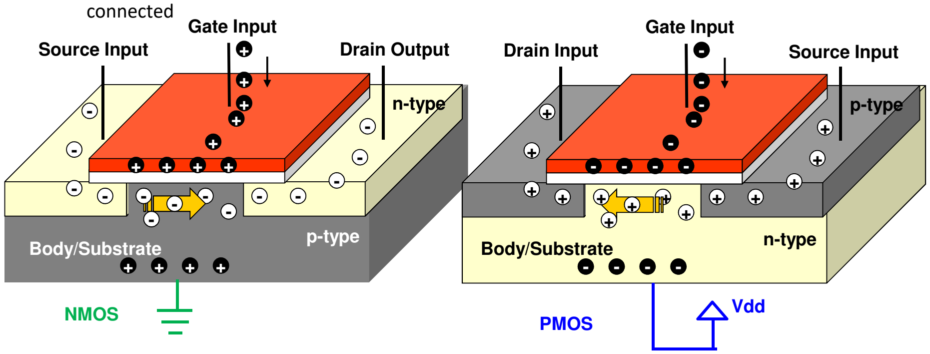
- Impurity atoms, i.e., donors or acceptors replace some silicon atoms in the crystal lattice
  - Donors: a valence of five e.g., phosphorus (P) or arsenic (As))
  - Acceptors: a valence of three, e.g., boron (B))
  - Remember these are electrically neutral (same # of protons/electrons), but are easily induced to donate or accept an electron under certain circumstances (i.e. under a voltage)
- If the donors or acceptors get ionized, each donor delivers an electron to the conduction band. Also each acceptor will capture an electron from valence band leaving a hole behind
  - Normally, at room temperature all donors (density N_D) and acceptors (concentration N_A) are ionized

A FEW QUICK NOTES

Body Terminal

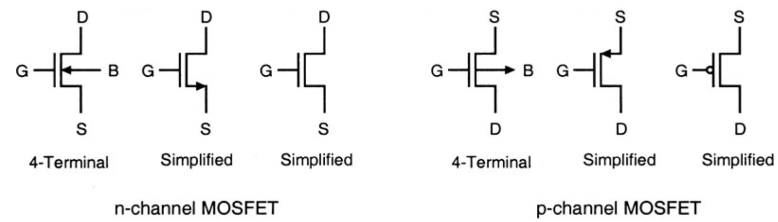
- Recall a PN junction acts like a diode and allows current flow when $V_{pn} > V_{thresh}$
- We don't want that current flow so we must **always maintain appropriate voltage to keep the "intrinsic" diodes in ____________**
  - Always keep the P-type area at a voltage _________ than the N-type
- For NMOS: Keep Body = _______; For PMOS: Keep Body = _________
  - We will often not show the body connection and assume it is appropriately connected





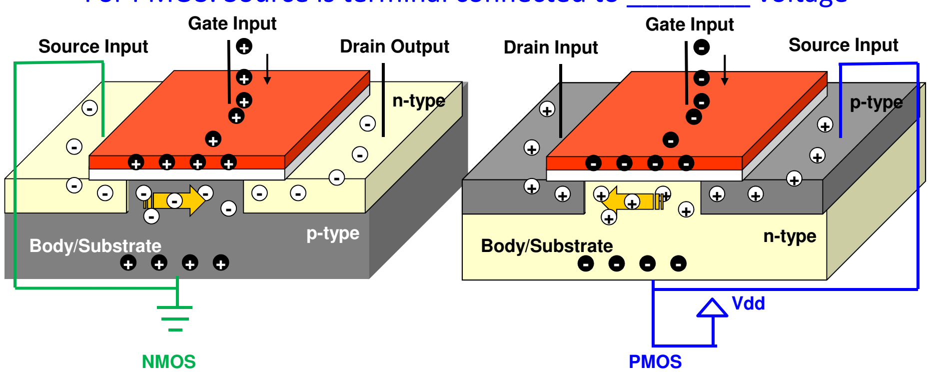
Conventions

- Since the source is always at the lowest voltage (for NMOS) and highest voltage (for PMOS) we generally define all voltages w.r.t. V_S
- Conventionally all terminal voltages are defined wrt V_S
- We also often draw our schematic symbols w/o showing the body terminal



Source or Drain

- Since MOSFETs are symmetric, which terminal is the source and which is the drain?
- It _______________________________!
- For NMOS: Source is terminal connected to _________ voltage
- For PMOS: Source is terminal connected to _________ voltage



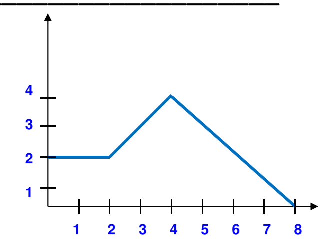
THE BASIC IDEA OF MOS OPERATION

NMOS vs. PMOS

- We will do all our analysis for NMOS but all the analogs hold true for PMOS (same equations but different constants and flipped n/p, etc.)
- Note: There are a LOT of equations we can and will show…
- …HOWEVER we will show you the main equations for the 3 different operating modes of a MOS transistor right now and most of the equations thereafter are just support for those primary ones and do not need to be memorized, etc.

Piece-wise Functions

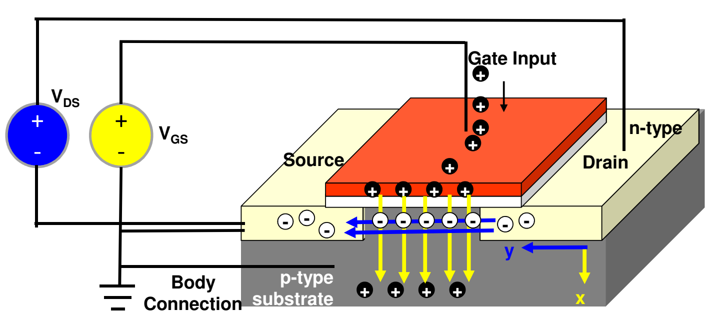
- How would I describe a function that has the following graph?
  - With _______________ function for the 3 _______ regions of operation
  - MOS transistors behave differently for 3 given input conditions, so we will describe those 3 cases with 3 ________________________



f(x) = {

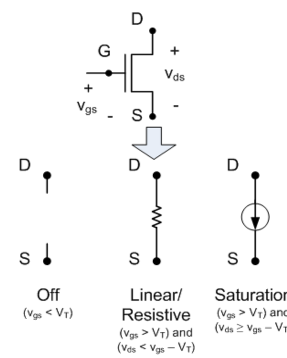
NMOS Transistor Physics

- Key idea: MOS operation relies on a voltage being developed in two _________________
  - From gate to source in the *x* dimension
  - From drain to source in the *y* dimension



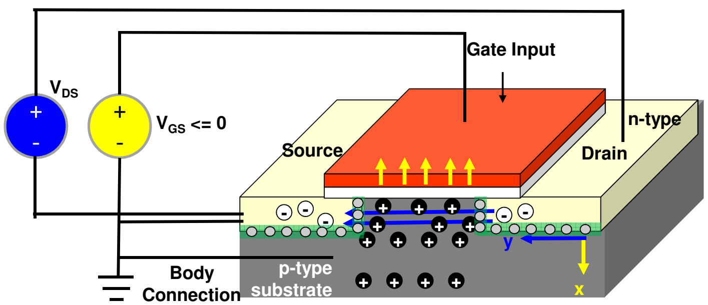
MOS Modes of Operation

- ______________
  - Transistor is off (drain to source is open circuit)
  - ____________ (Vt is whatever threshold voltage is needed to turn the transitor on…let's say 0.5-1.0V)
- ______________
  - Transistor is on and drain to source can be modeled as a _____________
  - __________ relationship between voltage/current
- ______________
  - Transistor is on and drain to source allows a _____________ of current despite _____________ voltage



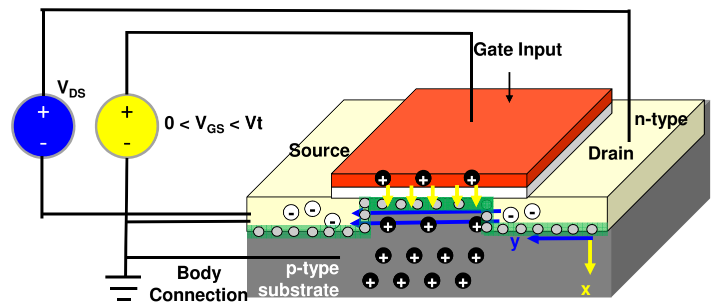
NMOS – Cutoff

- If ____________, then holes (p) accumulate at the surface preventing a channel from forming



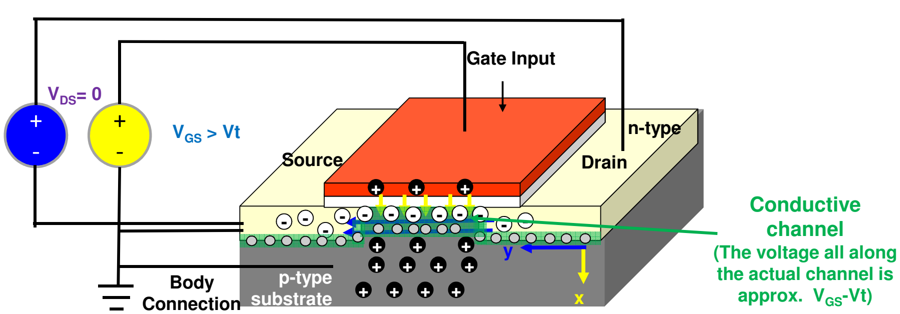
NMOS – Depletion

- As Vgs increases but is still ________ Vt, some electrons are induced into the _________ beneath the gate creating a _________ region (still no current can flow) but we are getting closer



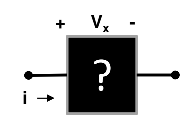
NMOS – Inversion

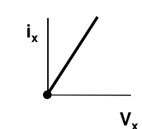
- As Vgs increases and reaches (and increases beyond) _____, enough electrons are induced into the channel
- We assume V_{DS} is _________ so there is no horizontal field to create a current flow across the channel, but the channel has now formed



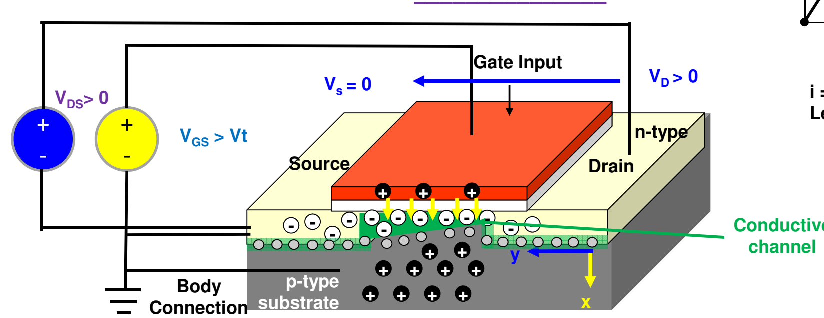
NMOS – Linear Mode

- So we have a conductive channel: ____________
- Now we increase _____ > 0 so current starts to flow
- The more we increase V_{DS} we get a ______ increase in the amount of current we can induce to flow
  - Wait! If I gave you a black box and showed that current through it grew linearly with voltage across it then…
  - …We can treat the black box like a ______________!



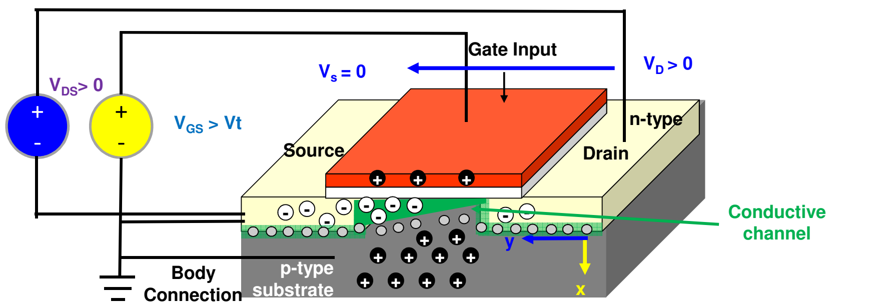


i = mV_x
Let m = ___



NMOS – Linear Mode

- What happens as we continue to increase V_{DS}?
- Notice the shape of the channel. It is ___________ near the drain? Why?
  - Because _____________ so there is more pull upward on the electrons near the drain than at the source
- As we increase V_{DS} the channel gets more and more narrow near the drain until it actually ___________________.



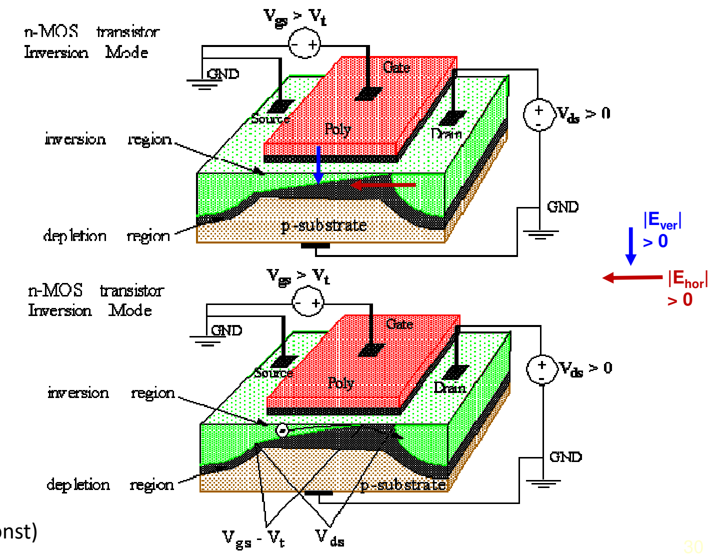
NMOS – Saturation

In **linear** region:

Vgs > Vt
and
0 < Vds < Vgs-Vt
(Vds ↑ => Ids ↑)

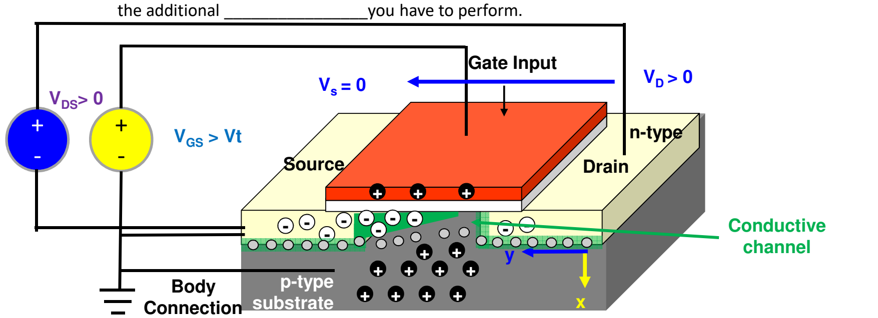
In **saturation** region:

Vgs > Vt
and
Vds > Vgs-Vt
(Vds ↑ => Ids = const)

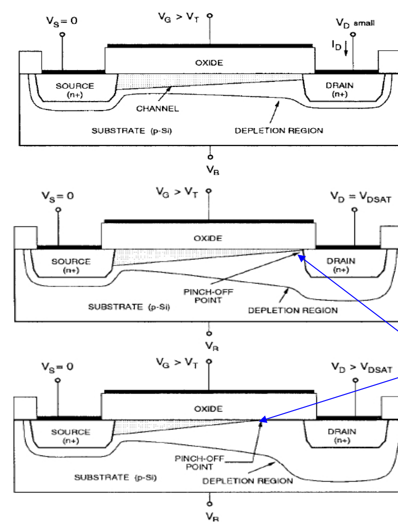


NMOS – Saturation

- Once ___________________ the channel starts to pinch off
- At this point an increase in V_{DS} (i.e. stronger electric field) does NOT induce ____________________________
  - The extra energy being applied is used to simply get the electrons across the depletion zone between the pinched off channel and the drain
  - And as we increase V_{DS} the channel pinches off even more meaning we have use more energy to get electrons across
  - Analogy: You can carry 15 items from one place to another in 10 minutes. I come to you and say, I'll give you a helper (increase V_{DS}) but you have to transport 30 items (i.e. it becomes more work/harder). Does the rate of transfer change? No, your additional help/energy is _________ on the additional _______________you have to perform.



nMOS Cross-sectional View Summary



Operating in the linear region

Another way to think about it: Vgs > Vgd so the channel is deeper near the source than the drain, but a continuous channel does exist

Operating at the edge of saturation

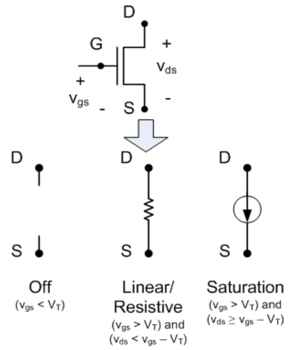
V_{DSAT} = Voltage where we crossed from linear (resistive) mode to saturation mode = Voltage at the pinchoff point = This is the voltage at which electrons in the channel are pulled into the drain by Vds rather than staying at the surface due to Vgs

Operating beyond saturation

Any increase in V_D beyond V_{DSAT} is dropped across the depletion region from drain to the pinchoff point causing the channel to experience the same voltage V_{DSAT} on one side and thus the same amount of current to flow through the channel

Summary of MOS Transistor Modes

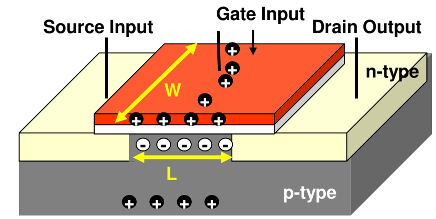
- MOS transistor (Ids/Vds relationship) can be modeled differently based on different operating conditions
  - Open circuit (off)
  - As a simple resistor between Drain & Source
  - As a constant current source between Drain & Source
  - Note: $K_n = \frac{\varepsilon_{ox}}{t_{ox}}\mu_n$ (K' = K_N for nmos, K_P for pmos)



Mode	Condition	Ids, Vds Relationship
Off	$v_{gs} < V_T$	$I_{ds} = 0$
Resistive	$v_{gs} > V_T$ and $v_{ds} < v_{gs} - V_T$	$I_{ds} = \frac{1}{2}K'\left(\frac{W}{L}\right)\left[2(v_{gs} - V_T)V_{ds} - {V_{ds}}^2\right]$
Saturation	$v_{gs} > V_T$ and $v_{ds} \geq v_{gs} - V_T$	$I_{ds} = \frac{1}{2}K'\left(\frac{W}{L}\right)\left[(v_{gs} - V_T)^2\right]$

Getting More Current to Flow

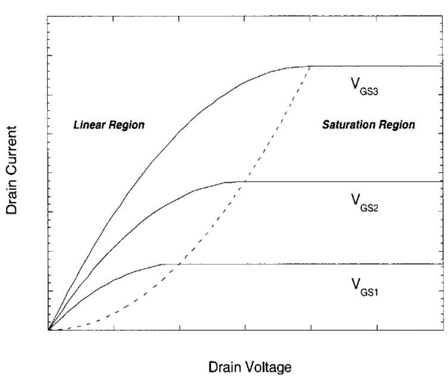
- Note: I_{ds} is proportional to K' (K_N or K_P) AND the ratio of ________
- For a transistor $K_N = C_{ox}\mu_n = \frac{\varepsilon_{ox}}{t_{ox}}\mu_n$ is some **intrinsic** (**we can't change it**) measurement of how well the transistor we built will conduct…
  - [Note: $K_P = C_{ox}\mu_P \neq K_N$]
- As a designer we can change W and L
  - W _ = Conductivity _ ;   L _ = Conductivity _
- As circuit designers, we can:
  - We can easily choose ______
  - Hard to change ________

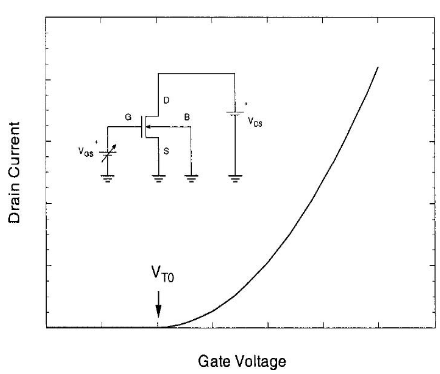


Changing ___ is something we will do a lot of in digital designs, mainly to influence _________ of a gate

Mode	Condition	Ids, Vds Relationship
Resistive	$v_{gs} > V_T$ and $v_{ds} < v_{gs} - V_T$	$I_{ds} = \frac{1}{2}K'\left(\frac{W}{L}\right)\left[2(v_{gs} - V_T)V_{ds} - {V_{ds}}^2\right]$
Saturation	$v_{gs} > V_T$ and $v_{ds} \geq v_{gs} - V_T$	$I_{ds} = \frac{1}{2}K'\left(\frac{W}{L}\right)\left[(v_{gs} - V_T)^2\right]$

nMOS I_D as a Function of V_{DS} and V_{GS}

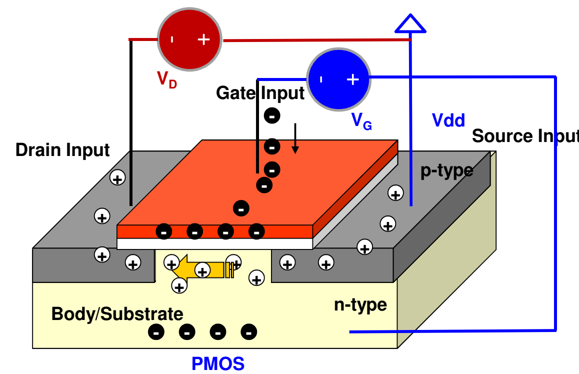




I_D vs V_{GS} for $V_{DS} > V_{DSAT}$

PMOS Operation

- Threshold voltage is now negative (e.g. -0.7V)
  - The gate has to be at a low enough voltage compared to the body to repel the electrons and attract free holes to create a conductive channel of holes



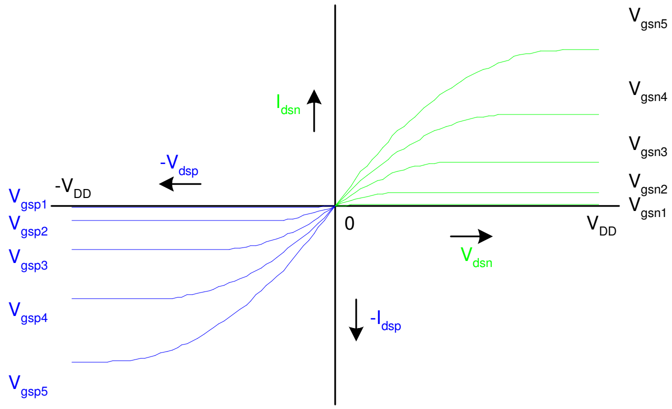
In cutoff:
Vgs > Vt

In linear region:
Vgs ≤ Vt
and
Vgs-Vt < Vds < 0

In saturation region:
Vgs ≤ Vt
and
Vds < Vgs-Vt

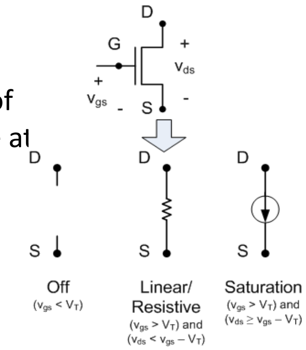
I-V Characteristics

- -Vdsp just means the drain is at a lower voltage than the source in the PMOS
- -Idsp just means the current is actually flowing from source to drain in the PMOS



Summary of NMOS or PMOS Transistors

- So that we don't get too caught up in the negative signs of PMOS transistors let us use the absolute value (ignore direction of current flow and sign of voltage) to arrive at one set of equations for either type
- We assume though:
  - NMOS: Vgs, Vt, Vds are all ______________ and current flows from D to S
  - PMOS: Vgs, Vt, Vds are all ______________ and current flows from S to D

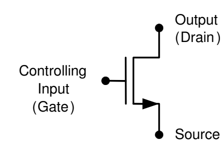


Mode	Condition	Ids, Vds Relationship
Off	$\lvert v_{gs}\rvert < \lvert V_T \rvert$	$\lvert I_{ds}\rvert = 0$
Resistive	$\lvert v_{gs}\rvert \geq \lvert V_T\rvert$ and $\lvert v_{ds}\rvert < \lvert v_{gs}\rvert - \lvert V_T\rvert$	$\lvert I_{ds}\rvert = \frac{1}{2}K'\left(\frac{W}{L}\right)\left[2(\lvert v_{gs}\rvert - \lvert V_T\rvert)\lvert V_{ds}\rvert - \lvert V_{ds}\rvert^2\right]$
Saturation	$\lvert v_{gs}\rvert \geq \lvert V_T\rvert$ and $\lvert v_{ds}\rvert \geq \lvert v_{gs}\rvert - \lvert V_T\rvert$	$\lvert I_{ds}\rvert = \frac{1}{2}K'\left(\frac{W}{L}\right)\left[(\lvert v_{gs}\rvert - \lvert V_T\rvert)^2\right]$

EXAMPLE DERIVATIONS

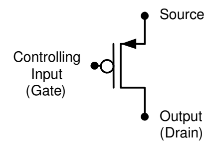
Example – NMOS Region Calculation

- V_t of an NMOS transistors is 0.35 v
- V_{DD} = 1.2v
- What are the conditions for the transistor to be
  - ON
  - In Linear region
  - In saturation region



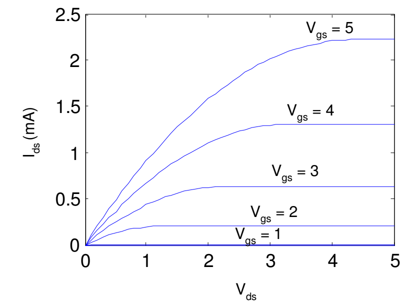
Example – PMOS Region Calculation

- V_t of a PMOS transistors is -0.35 v
- V_{DD} = 1.2v
- What are the conditions for the transistor to be
  - ON
  - In Linear region
  - In saturation region



Example – Current Calculation

- A 0.6 μm process from AMI semiconductor
  - t_{ox} = 100 angstroms (1 angstrom = 1E-10 m = 1E-8 cm)
  - ε_{ox} =3.9*8.85E-14 F/cm
  - μ = 350 cm²/V.s
  - V_t = 0.7 V
- Plot I_{ds} vs V_{ds}
  - V_{gs} = 0, 1, 2, 3, 4, 5
  - Use W/L = 4λ/2λ

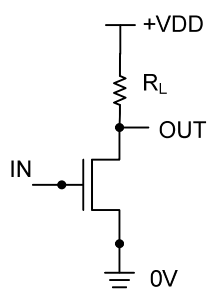


$$\beta = \mu C_{ox}\frac{W}{L} = (350)\left(\frac{3.9 \bullet 8.85 \cdot 10^{-14}}{100 \cdot 10^{-8}}\right)\left(\frac{W}{L}\right) = 120\frac{W}{L}\mu A/V^2$$

Calculate Vout

- Given V_T = 0.5, V_{DD} = V_{GS} = 3V, K_N = 240 μA/V², W/L = 1, and R_L = 10KΩ
  - Note: Vout = V_{DS} and thus V_L = V_{DD}-V_{DS}
- Consider what mode the transistor is in, then setup a KCL equation at the output…
  - We know V_{GS}-V_T is 2.5 while VDS (=Vout) is very likely less-than 2.5 since we have a voltage divider and R_L = 10K with most of the 3V dropped across R_L leaving Vout to be small…Thus we are in ___________ mode

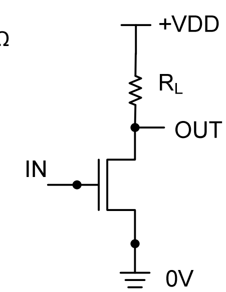
$$I_{R_L} = I_{DS}$$



Mode	Condition	Ids, Vds Relationship
Resistive	$\lvert v_{gs}\rvert \ge \lvert V_T\rvert$ and $\lvert v_{ds}\rvert < \lvert v_{gs}\rvert - \lvert V_T\rvert$	$\lvert I_{ds}\rvert = \frac{1}{2}K'\left(\frac{W}{L}\right)\left[2(\lvert v_{gs}\rvert - \lvert V_T\rvert)\lvert V_{ds}\rvert - \lvert V_{ds}\rvert^2\right]$
Saturation	$\lvert v_{gs}\rvert \ge \lvert V_T\rvert$ and $\lvert v_{ds}\rvert \ge \lvert v_{gs}\rvert - \lvert V_T\rvert$	$\lvert I_{ds}\rvert = \frac{1}{2}K'\left(\frac{W}{L}\right)\left[(\lvert v_{gs}\rvert - \lvert V_T\rvert)^2\right]$

Calculate Vout

- Given V_T = 0.5, V_{DD} = V_{GS} = 3V, K_N = 240 μA/V², W/L = 1, and R_L = 10KΩ
  - Note: Vout = V_{DS} and thus V_L = V_{DD}-V_{DS}
- Finish solving the previous problem and then consider the change in the answer if the Width of the transistor is doubled



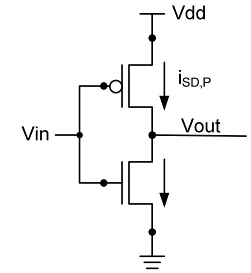
Mode	Condition	Ids, Vds Relationship
Resistive	$\lvert v_{gs}\rvert \ge \lvert V_T\rvert$ and $\lvert v_{ds}\rvert < \lvert v_{gs}\rvert - \lvert V_T\rvert$	$\lvert I_{ds}\rvert = \frac{1}{2}K'\left(\frac{W}{L}\right)\left[2(\lvert v_{gs}\rvert - \lvert V_T\rvert)\lvert V_{ds}\rvert - \lvert V_{ds}\rvert^2\right]$
Saturation	$\lvert v_{gs}\rvert \ge \lvert V_T\rvert$ and $\lvert v_{ds}\rvert \ge \lvert v_{gs}\rvert - \lvert V_T\rvert$	$\lvert I_{ds}\rvert = \frac{1}{2}K'\left(\frac{W}{L}\right)\left[(\lvert v_{gs}\rvert - \lvert V_T\rvert)^2\right]$

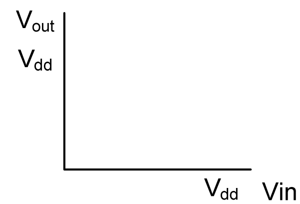
Calculating "DC" (Constant) Voltage Input/Output Relationship

STATIC INVERTER ANALYSIS

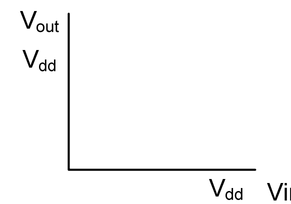
Recall the Inverter

- General problem: Given Vin and other parameters calculate Vout
- Take a moment and think: What should the plot of Vin vs. Vout look like
- How can we calculate Vout, given Vin?





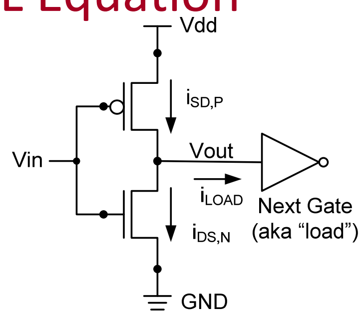
Ideal (CMOS comes close)

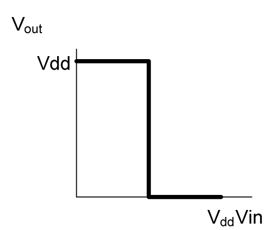


Other Implementations may be non-ideal

Step 1: Setup a KCL Equation

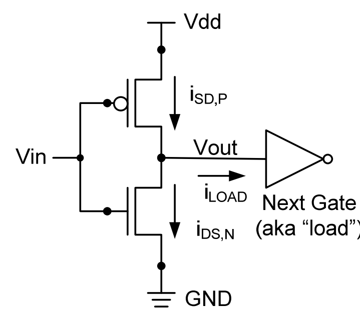
- Calculating the static ('steady state') Vin/Vout relationship?
- Use equations for MOS transistors by recognizing the following:
  - ________________ **according to KCL**
  - I_{LOAD} = 0 (next gate = no current flow)
  - So ___________
    - The current through the PMOS must equal the current through the NMOS (we can set them equal) and we have equations for the currents ($|I_{DS,P}|$ and $|I_{DS,N}|$)

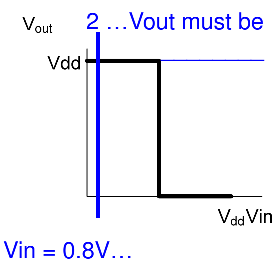




Step 2: Use Educated Guess for Modes of Operation

- But what mode are they in?
  - $V_{GS,N}$ = ____________________
  - $V_{DS,N}$ = ____________________
  - $V_{GS,P}$ = ____________________________
- Given the assumptions…
  - $V_{T,N} = V_{T,P} = 0.5V$; Vdd = 3.0V; $k_n = 2k_p$; L=1; W_n = 1; W_p = 2; and Vin = 0.8V
- Then use the Vin/Vout relationship and the given value of Vin to make an educated guess
  - Since Vin is low, Vout should be __________
  - $V_{GS,N}$ – Vt = _____ and $V_{DS,N}$ = close to Vdd
    - NMOS is in _____
  - $|V_{GS,P}|-|V_T|$ = __________________ while $|V_{DS,P}|$ = 3V - ____________ = ________
    - PMOS is in ___________





Step 3: Setup Eqn & Solve for Vout

- Use the current equations for each transistor in its appropriate mode and solve for Vout

$$|I_{ds,p,LIN}| = \frac{1}{2}K_P'\left(\frac{W}{L}\right)_P\left[2\left(|v_{gs,p}| - |V_{T,p}|\right)|V_{ds,p}| - |V_{ds,p}|^2\right] =$$

$$|I_{ds,n,SAT}| = \frac{1}{2}K_N'\left(\frac{W}{L}\right)_N\left[\left(|v_{gs,n}| - |V_{T,n}|\right)^2\right]$$

$$\frac{1}{2}K_P'\left(\frac{W}{L}\right)_P\left[2\left(|v_{gs,p}| - |V_{T,p}|\right)|V_{ds,p}| - |V_{ds,p}|^2\right] = \frac{1}{2}K_N'\left(\frac{W}{L}\right)_N\left[\left(|v_{gs,n}| - |V_{T,n}|\right)^2\right]$$

$$\frac{1}{2}K_P'\left(\frac{2W}{L}\right)_N[2(|V_{dd} - v_{in}| - |0.5|)|V_{dd} - v_{out}| - |V_{dd} - v_{out}|^2] = \frac{1}{2}2K_P'\left(\frac{W}{L}\right)_N[(|v_{in}| - |0.5|)^2]$$

$$[2(|3 - 0.8| - |0.5|)|3 - v_{out}| - |3 - v_{out}|^2] = [(|0.8| - |0.5|)^2]$$

$$[3.4 * |3 - v_{out}| - |3 - v_{out}|^2] = 0.09$$

…continue on to solve for Vout