Spiral 2-6

Semiconductor Material
MOS Theory

Learning Outcomes

- I understand why a diode conducts current under forward bias but does not under reverse bias
- I understand the three modes of operation of a MOS transistor and the conditions associated with each mode
- I can analyze circuits containing MOS transistors to find current and voltage values by first determining the mode of operation and then applying the appropriate equations

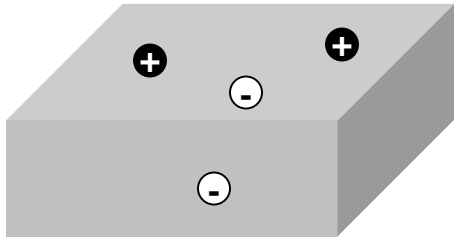
Current, Voltage, & Resistors

- Kirchoff's Current Law
  - Sum of current into a node is equal to current coming out of a node
- Kirchoff's Voltage Law
  - Sum of voltages around a loop is 0
- Ohm's Law (only applies to resistors or devices that "act" like a resistor)
  - I = V/R, R = V/I, or V = IR
  - Note: For a resistor, current and voltage are linearly related with R as the slope

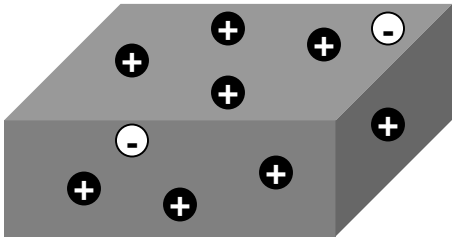
DIODES

Semiconductor Material

- Semiconductor material is not a great conductor material in its pure form
  - Small amount of free charge
- Can be implanted ("doped") with other elements (e.g. boron or arsenic) to be more conductive
  - Increases the amount of free charge

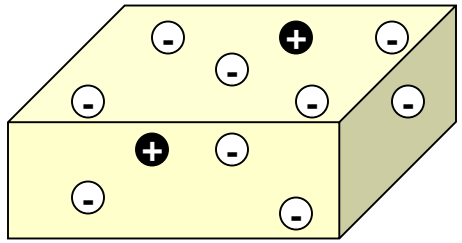


Pure Silicon



P-Type Silicon
(Doped with boron)

Electron acceptors

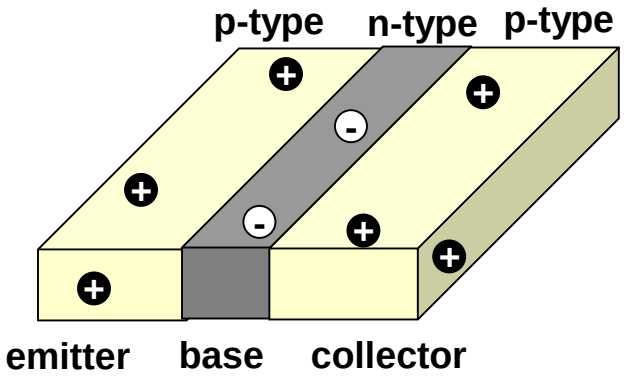


N-Type Silicon
(Doped with arsenic)

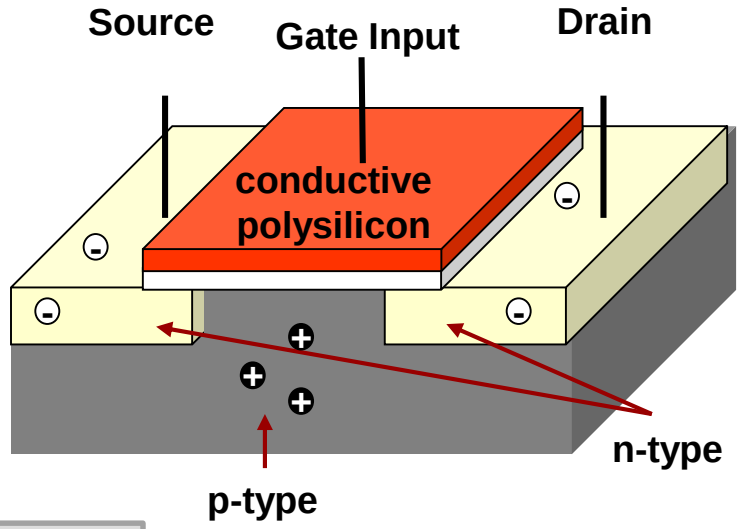
Electron donors

Transistor Types

- Bipolar Junction Transistors (BJT)
  - npn or pnp silicon structure
  - Small current into very thin base layer controls large currents between emitter and collector
  - However the fact that it requires a current into the base means it burns power (P = I*V) and thus limits how many we can integrate on a chip (i.e. density)
- Metal Oxide Semiconductor Field Effect Transistors
  - nMOS and pMOS MOSFETS
  - Voltage applied to insulated gate controls current between source and drain
    - Gate input requires no constant current…thus low power!



npn BJT

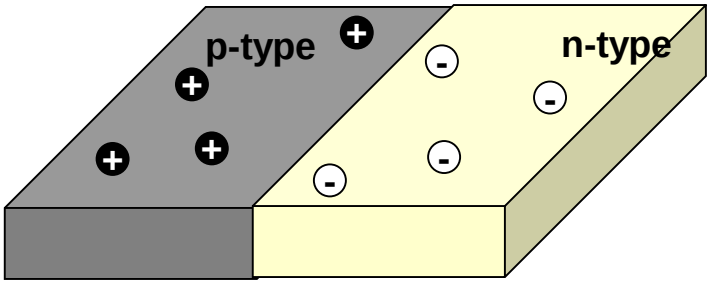


N-type MOSFET

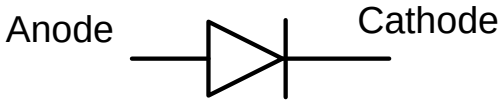
We will focus on MOSFET in this class

PN Junction Diode

- Our understanding of how a transistor works will start by analyzing a simpler device: a diode
- A diode can be formed by simply butting up some p-type and n-type material together



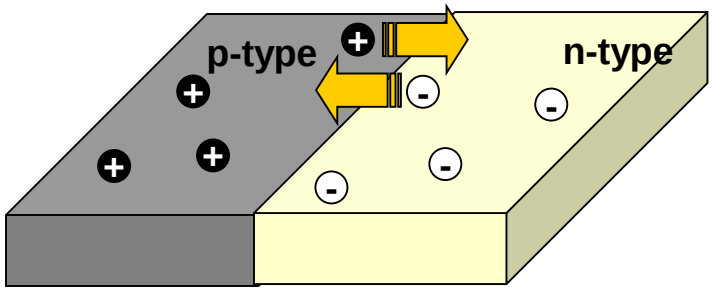
Physical view



Schematic symbol of a diode

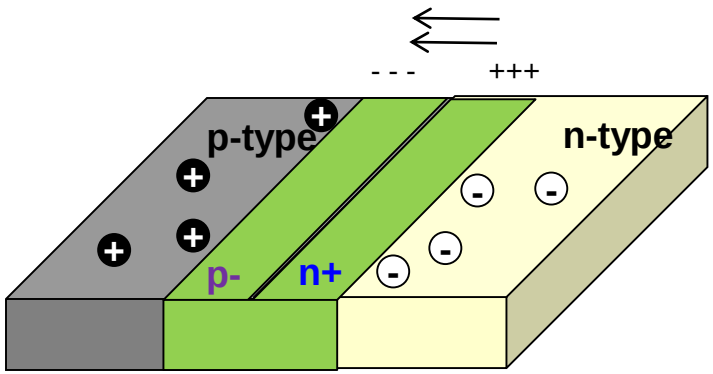
The PN Junction

- When we join the two substances the free electrons at the junction will combine with the nearby free holes in a "loose" bond
- This has two effects:
  - Around the junction there are no more free charges (they've all combined) creating a **depletion region**
  - Now remember the dopants in n- and p-type material were still neutrally charged (same # of protons/electrons). So this migration has actually created ions and thus an electric field (and thus voltage) in the opposite direction



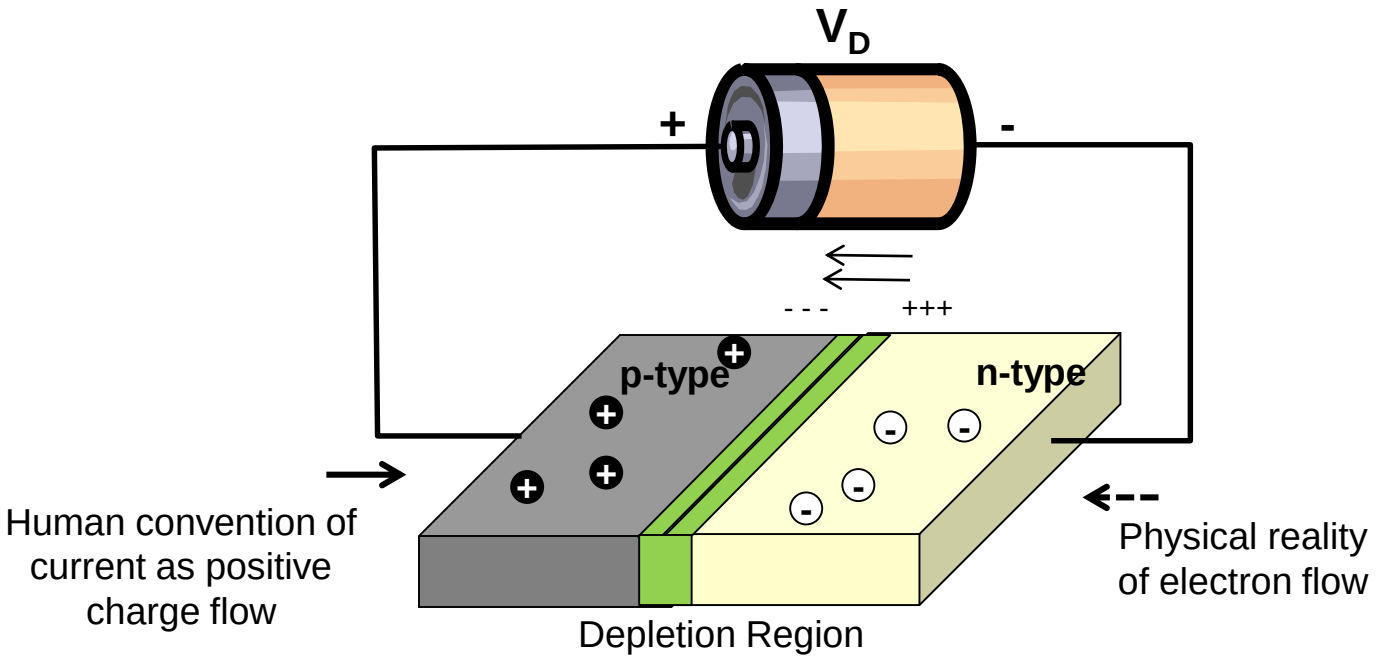
Depletion Region

- Depletion region has no/few free or mobile charge
- A small voltage is induced due to this recombination
  - N-type material LOST an electron leaving a positive ion
  - P-Type material LOST a hole (GAINED an electron) leaving a negative ion
  - The voltage is in the opposite direction



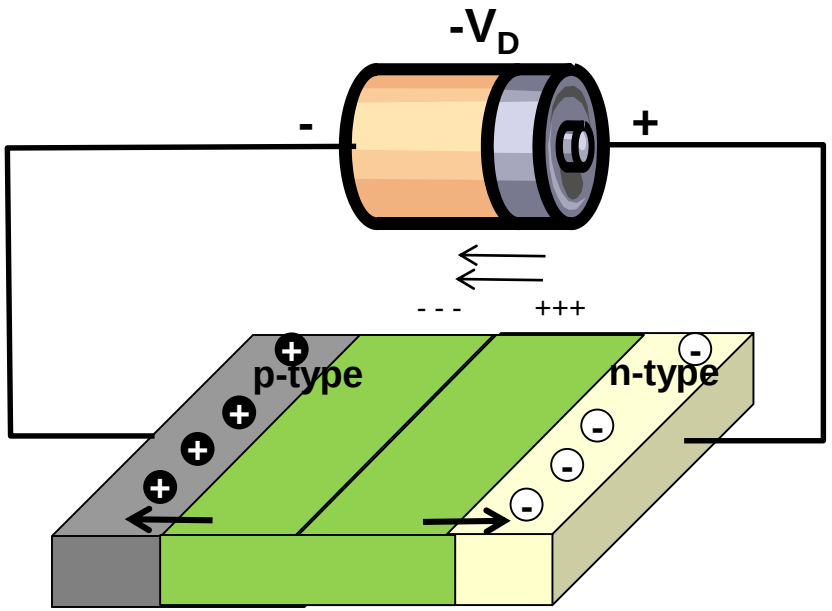
Forward Bias

- Now let's place an external positive voltage source across the diode
  - Holes and electrons are pushed toward each other and reduce the depletion region
  - If the external voltage is high enough the charges will have enough energy to overcome the gap and start flowing through the diode
  - The positive external voltage needed to overcome the depletion region is known as the Threshold Voltage



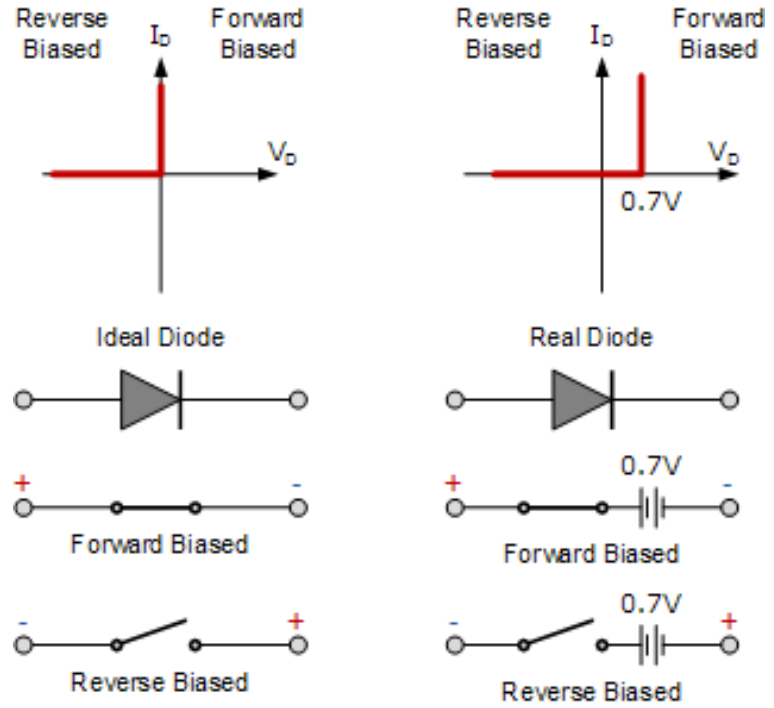
Reverse Bias

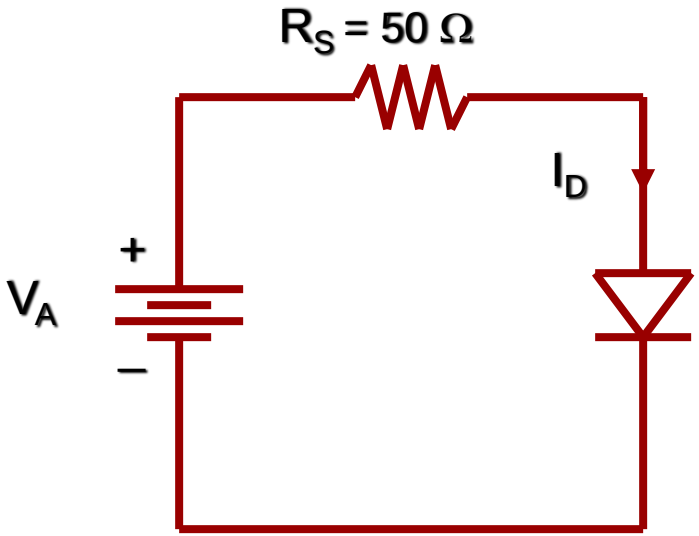
- Now let's place an external negative voltage source across the diode
  - Holes and electrons are attracted to the voltage source terminal (pulled away from the depletion area making the depletion area expand)
  - No current is flowing across the junction because both holes and electrons are attracted in opposite directions



Ideal Diode

- A perfect diode would ideally allow current to flow in one direction only
- It would therefore be a perfect conductor in one direction (forward bias) and a perfect insulator in the other direction (reverse bias)
- Example: Determine the value of ID if a) VA = 5 volts (forward bias) and b) VD = -5 volts (reverse bias)
  - Ideal model:
    - a) $I_D = V_A/R_S = 5\ V / 50\ \Omega = 100\ mA$
    - b) Diode is in reverse bias and is acting like a perfect insulator, therefore no current can flow and $I_D = 0$
  - More realistic:
    - a) $I_D = (V_A - 0.7v)/R_S = 86\ mA$
    - b) $I_D = 0$

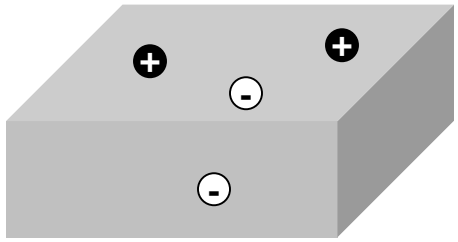




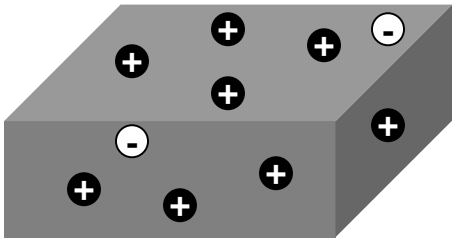
TRANSISTORS

Carrier Concentration

- Even silicon has some amount of free electrons (n) and holes (p)
  - We refer to this as the intrinsic carrier concentration
  - Note: n = p since a free electron leaves a hole behind
- When we add dopants we change the carrier concentration
  - N_A and N_D is the concentration of acceptors and donors respectively
  - Note: $N_A >> p$ and $N_D >> n$

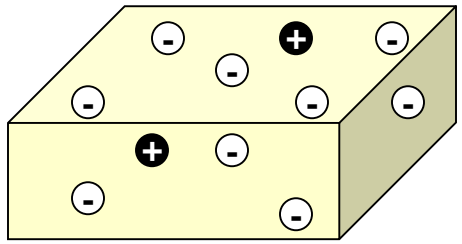


Pure Silicon



P-Type Silicon
(Doped with boron)

Electron acceptors



N-Type Silicon
(Doped with arsenic)

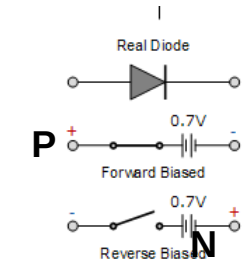
Electron donors

Doped Valence and Conduction Bands

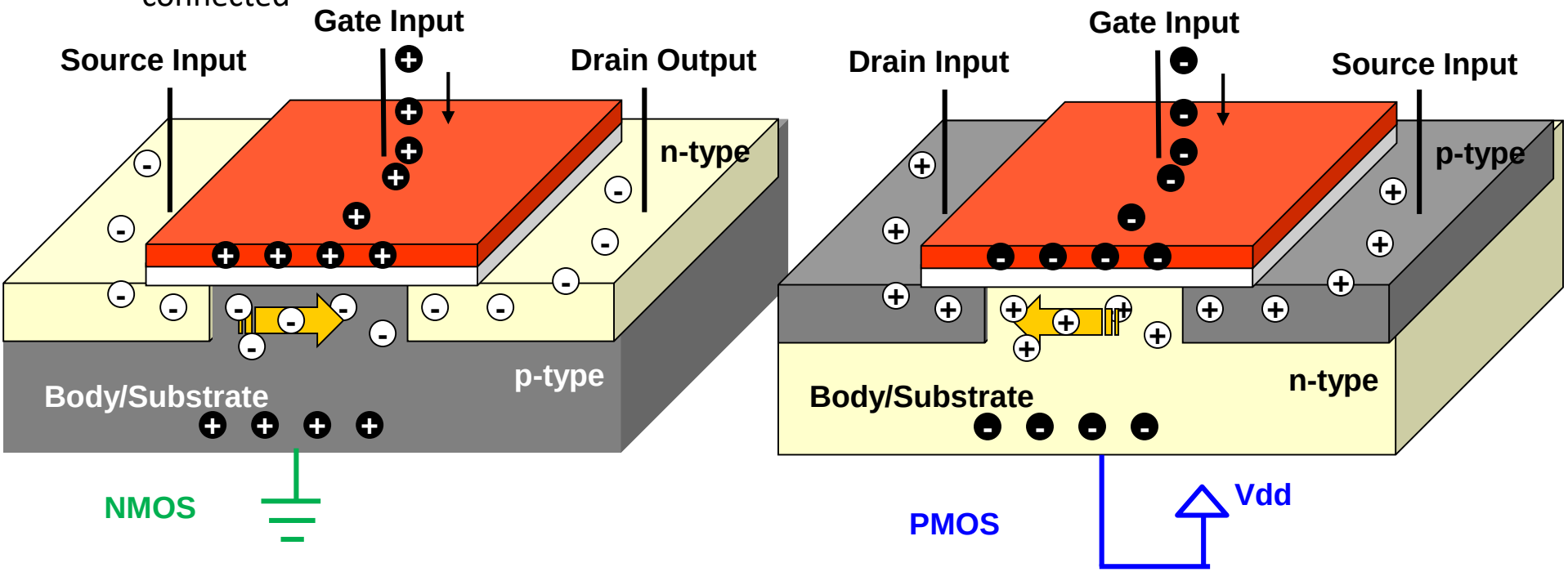
- Impurity atoms, i.e., donors or acceptors replace some silicon atoms in the crystal lattice
  - Donors: a valence of five e.g., phosphorus (P) or arsenic (As))
  - Acceptors: a valence of three, e.g., boron (B))
  - Remember these are electrically neutral (same # of protons/electrons), but are easily induced to donate or accept an electron under certain circumstances (i.e. under a voltage)
- If the donors or acceptors get ionized, each donor delivers an electron to the conduction band. Also each acceptor will capture an electron from valence band leaving a hole behind
  - Normally, at room temperature all donors (density ND) and acceptors (concentration NA) are ionized

A FEW QUICK NOTES

Body Terminal

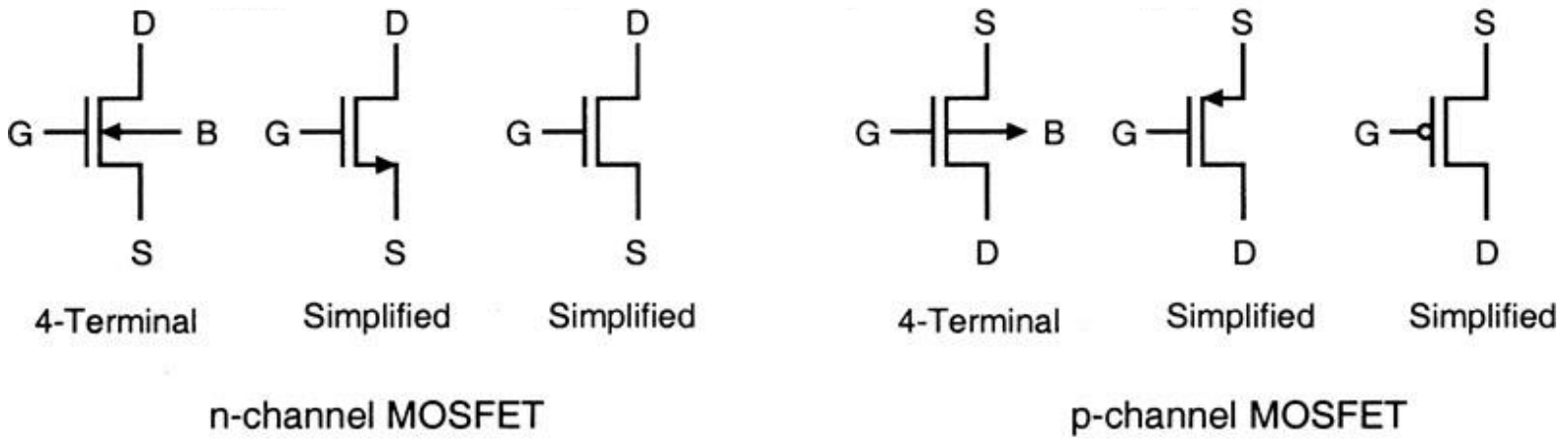


- Recall a PN junction acts like a diode and allows current flow when $V_{pn} > V_{thresh}$
- We don't want that current flow so we must **always maintain appropriate voltage to keep the "intrinsic" diodes in reverse bias**
  - Always keep the P-type area at a voltage lower than the N-type
- For NMOS: Keep Body = GND; For PMOS: Keep Body = Vdd
  - We will often not show the body connection and assume it is appropriately connected



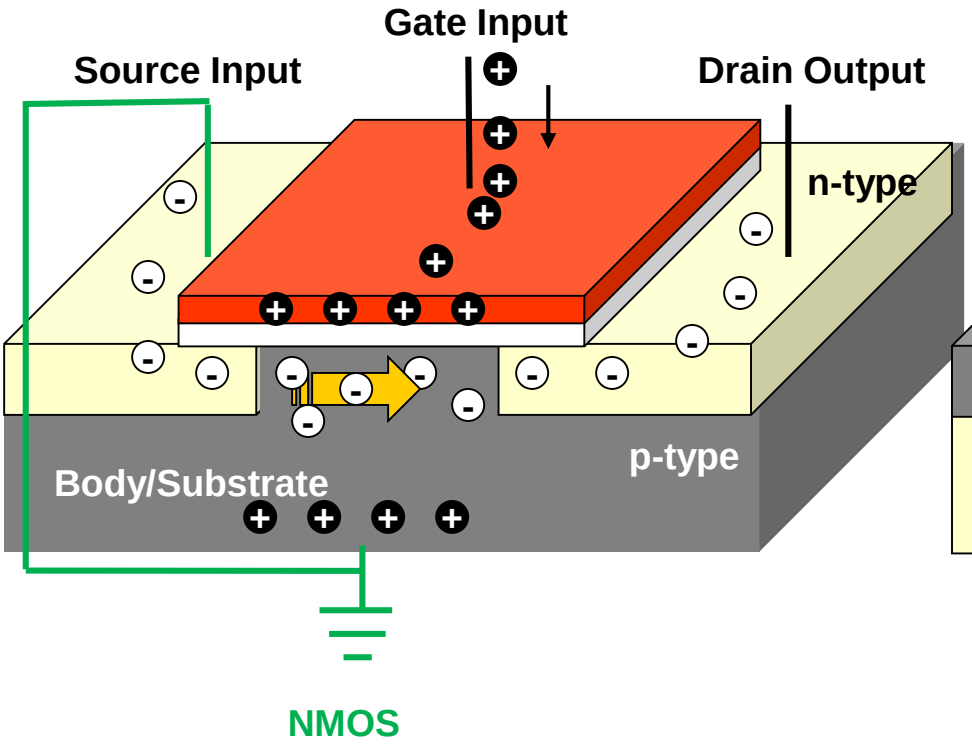
Conventions

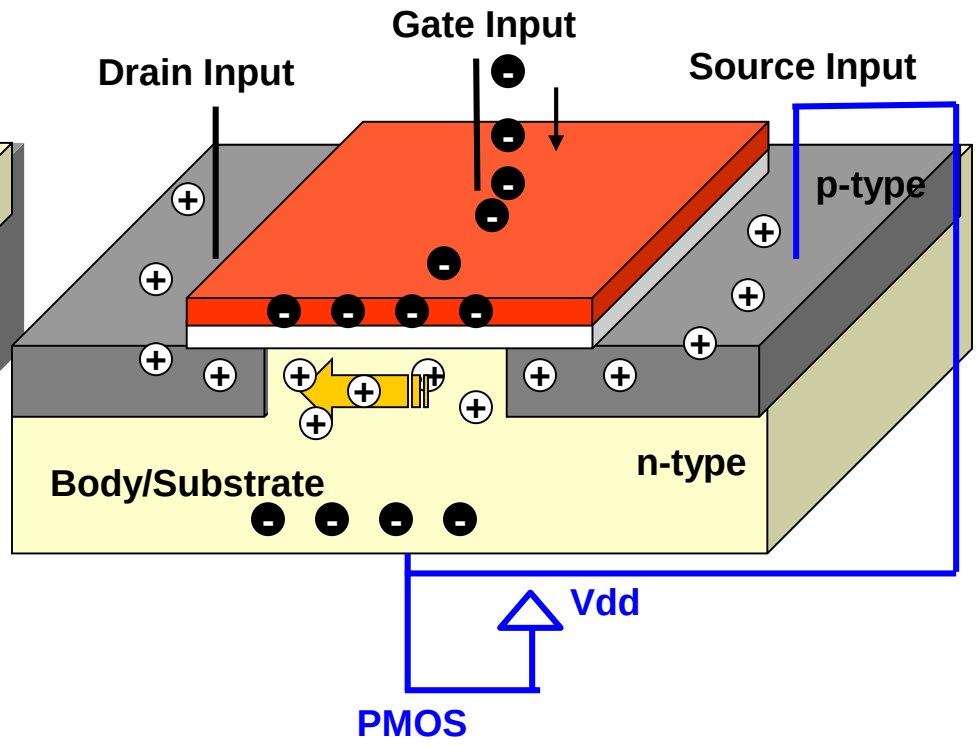
- Since the source is always at the lowest voltage (for NMOS) and highest voltage (for PMOS) we generally define all voltages w.r.t. V_S
- Conventionally all terminal voltages are defined wrt V_S
- We also often draw our schematic symbols w/o showing the body terminal



Source or Drain

- Since MOSFETs are symmetric, which terminal is the source and which is the drain?
- It depends on how we connect it!
- For NMOS: Source is terminal connected to lower voltage
- For PMOS: Source is terminal connected to higher voltage





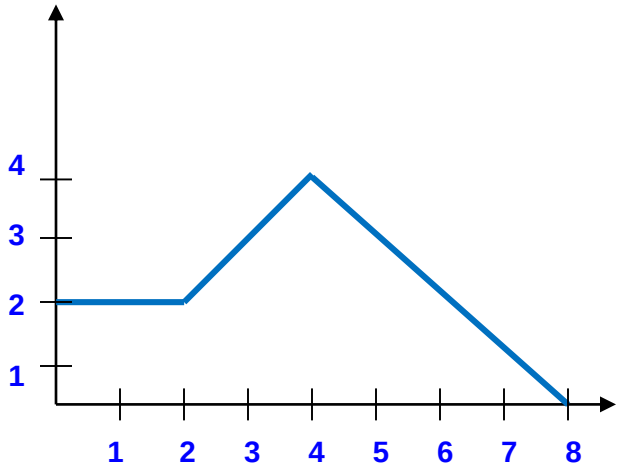
THE BASIC IDEA OF MOS OPERATION

NMOS vs. PMOS

- We will do all our analysis for NMOS but all the analogs hold true for PMOS (same equations but different constants and flipped n/p, etc.)
- Note: There are a LOT of equations we can and will show…
- …HOWEVER we will show you the main equations for the 3 different operating modes of a MOS transistor right now and most of the equations thereafter are just support for those primary ones and do not need to be memorized, etc.

Piece-wise Functions

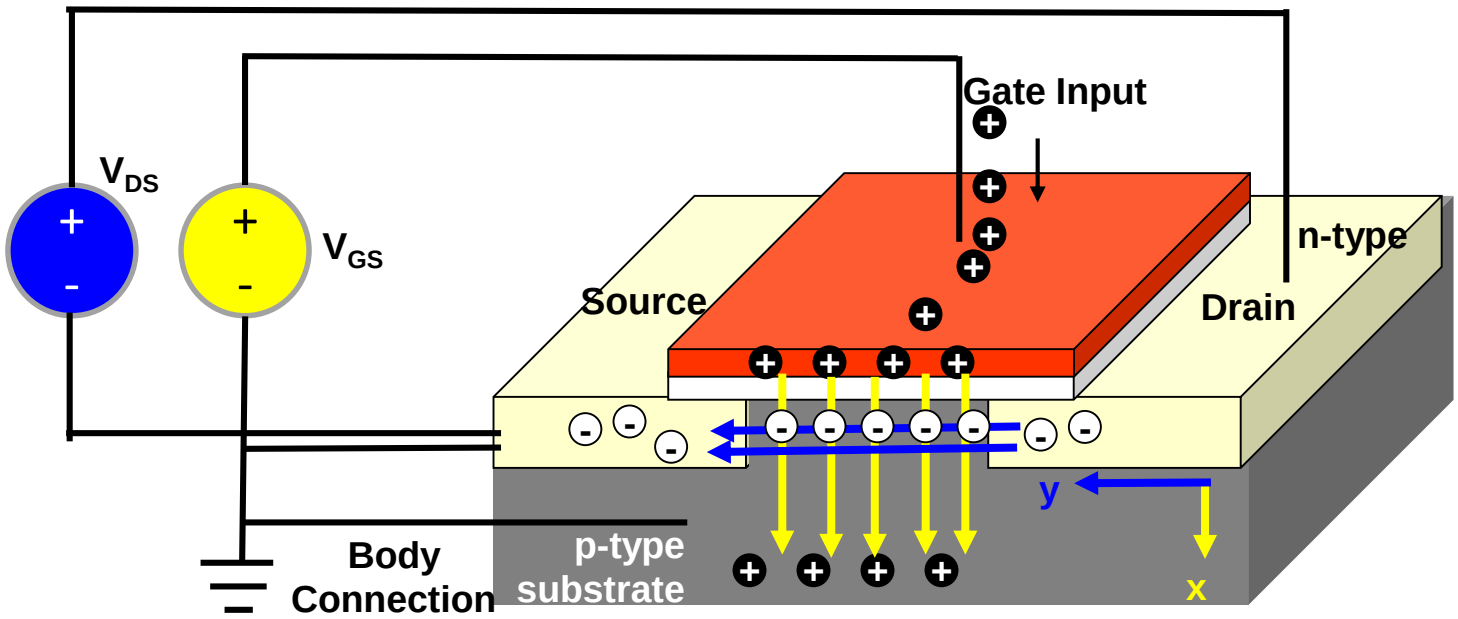
- How would I describe a function that has the following graph?
  - With 3 separate function for the 3 distinct regions of operation
  - MOS transistors behave differently for 3 given input conditions, so we will describe those 3 cases with 3 different functions



$$f(x) = \begin{cases} 2, & x < 2 \\ x, & 2 <= x < 4 \\ -x, & 4 <= x < 8 \end{cases}$$

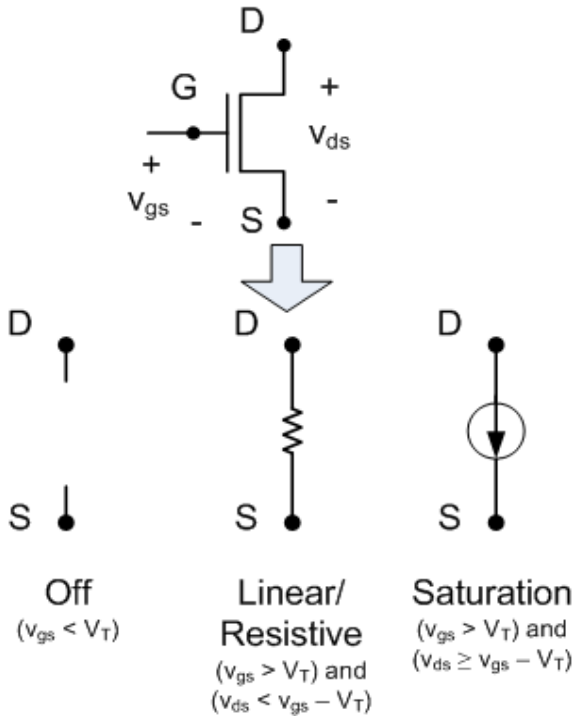
NMOS Transistor Physics

- Key idea: MOS operation relies on a voltage being developed in two dimensions
  - From gate to source in the *x* dimension
  - From drain to source in the *y* dimension



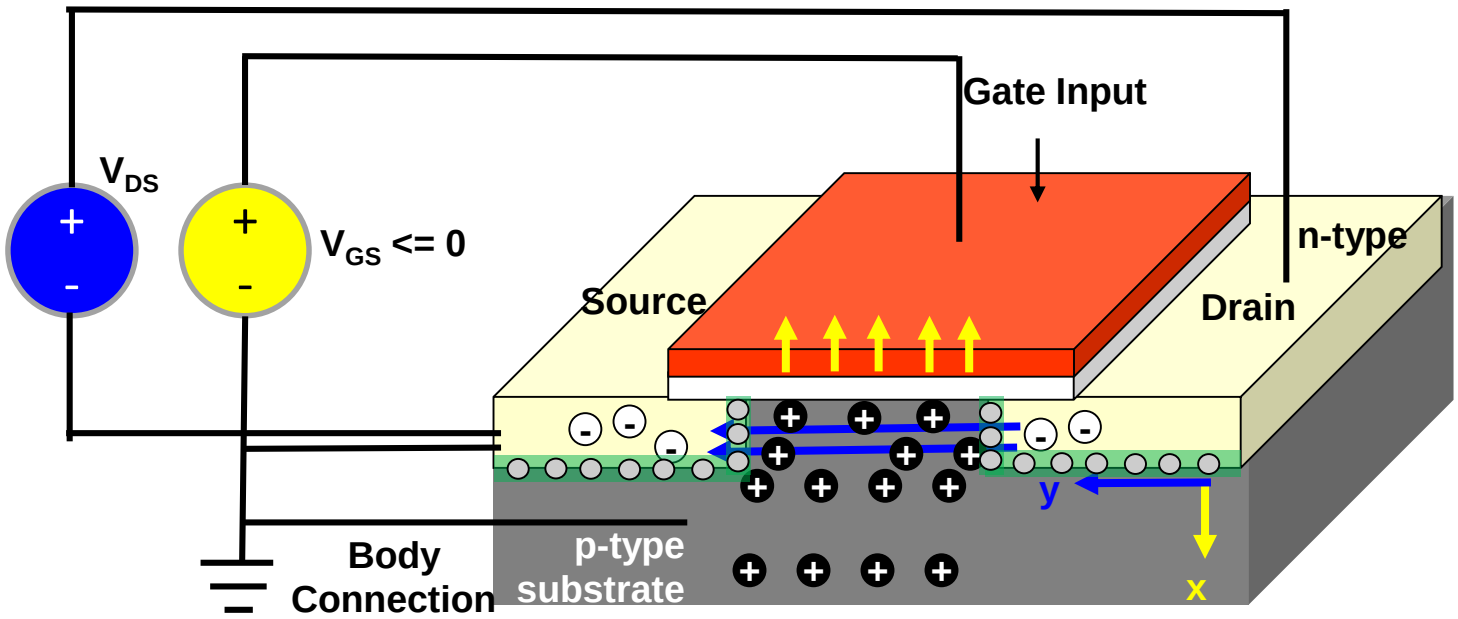
MOS Modes of Operation

- Cutoff
  - Transistor is off (drain to source is open circuit)
  - $V_{GS} < V_T$ (Vt is whatever threshold voltage is needed to turn the transitor on…let's say 0.5-1.0V)
- Linear
  - Transistor is on and drain to source can be modeled as a resistor
  - Linear relationship between voltage/current
- Saturation
  - Transistor is on and drain to source allows a fixed amount of current despite increased voltage



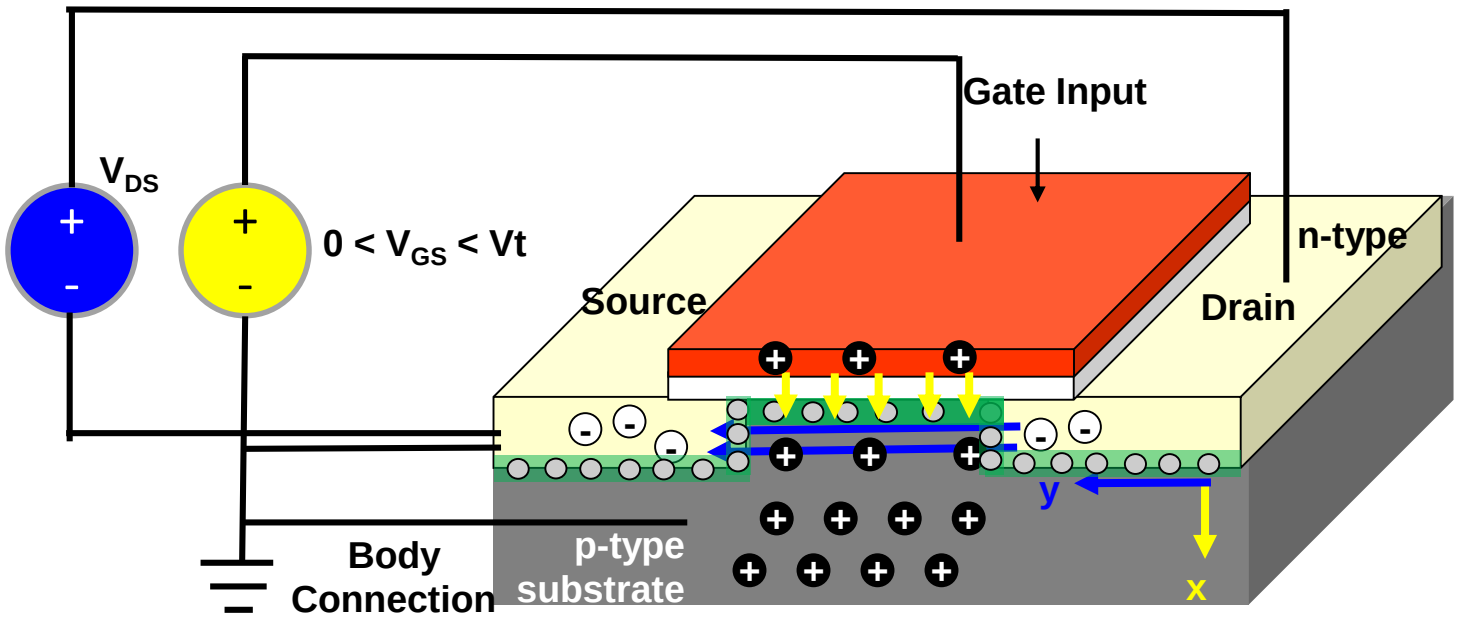
NMOS – Cutoff

- If Vgs <= 0, then holes (p) accumulate at the surface preventing a channel from forming



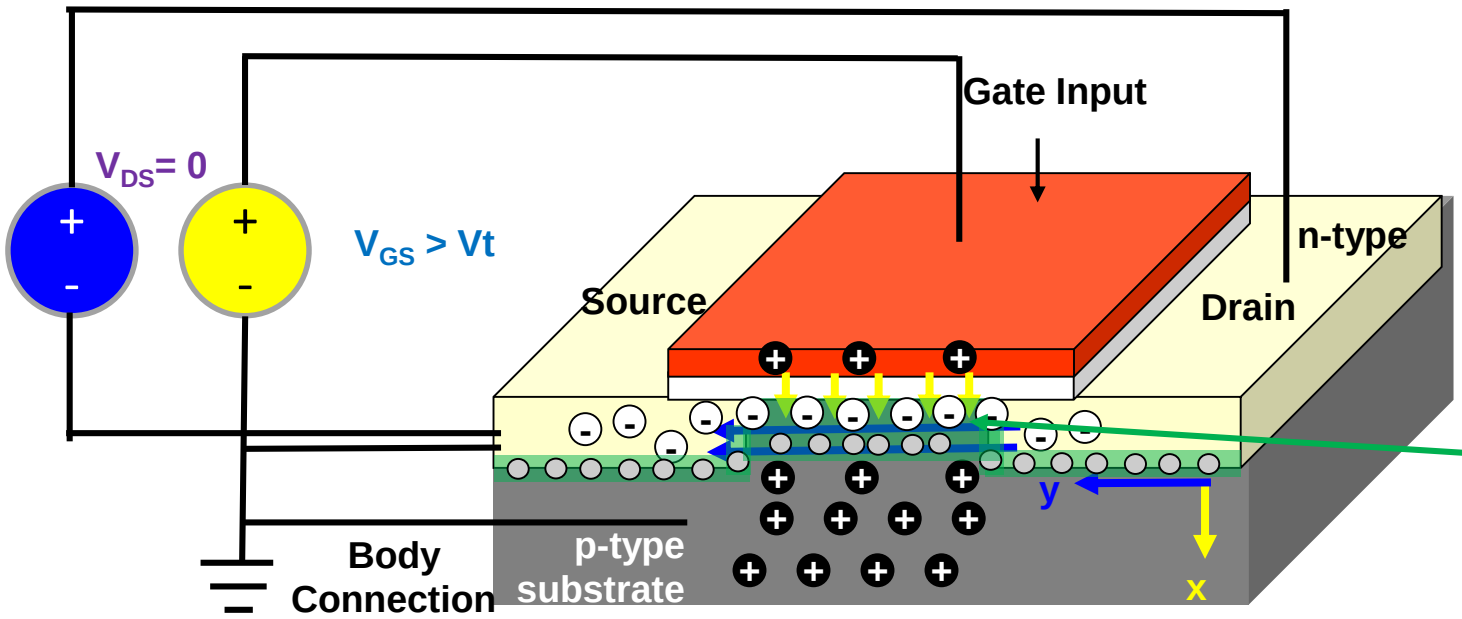
NMOS – Depletion

- As Vgs increases but is still below Vt, some electrons are induced into the channel beneath the gate creating a depletion region (still no current can flow) but we are getting closer



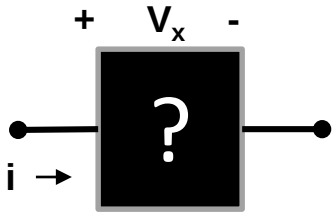
NMOS – Inversion

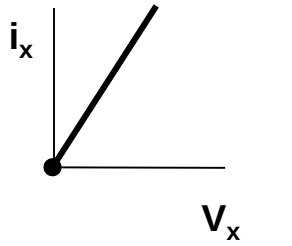
- As Vgs increases and reaches (and increases beyond) V_T, enough electrons are induced into the channel
- We assume V_{DS} is still 0 so there is no horizontal field to create a current flow across the channel, but the channel has now formed



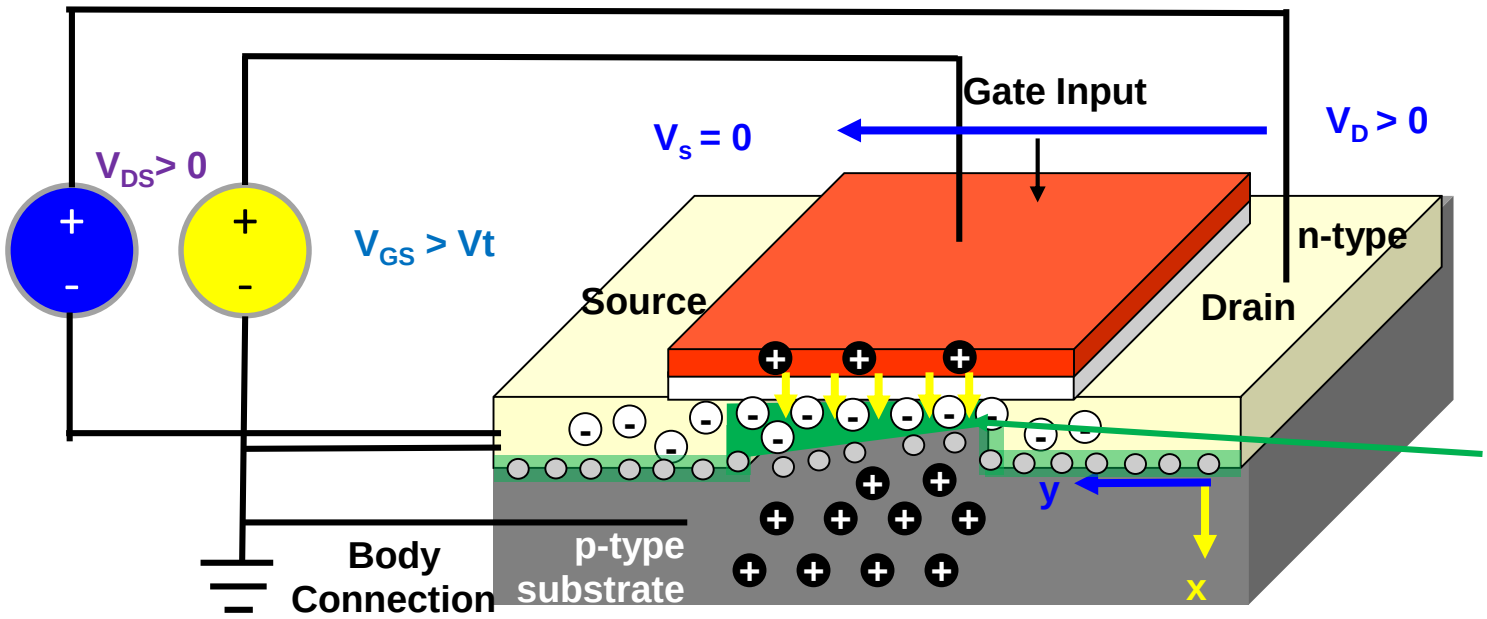
NMOS – Linear Mode

- So we have a conductive channel: Vgs > V_T
- Now we increase $V_{DS} > 0$ so current starts to flow
- The more we increase VDS we get a linear increase in the amount of current we can induce to flow
  - Wait! If I gave you a black box and showed that current through it grew linearly with voltage across it then…
  - …We can treat the black box like a **resistor**!



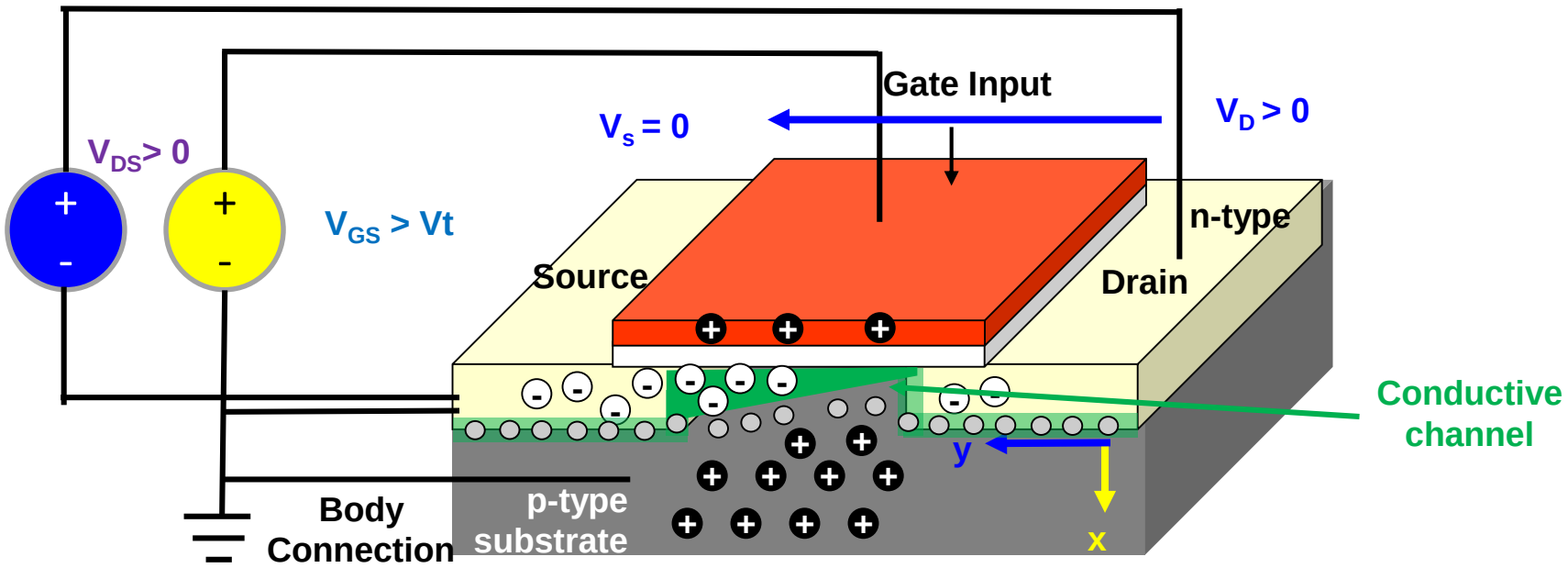


$i = mV_x$
Let m = ____



NMOS – Linear Mode

- What happens as we continue to increase V_{DS}?
- Notice the shape of the channel. It is narrower near the drain? Why?
  - Because V_D is positive so there is more pull upward on the electrons near the drain than at the source
- As we increase V_{DS} the channel gets more and more narrow near the drain until it actually pinches off.



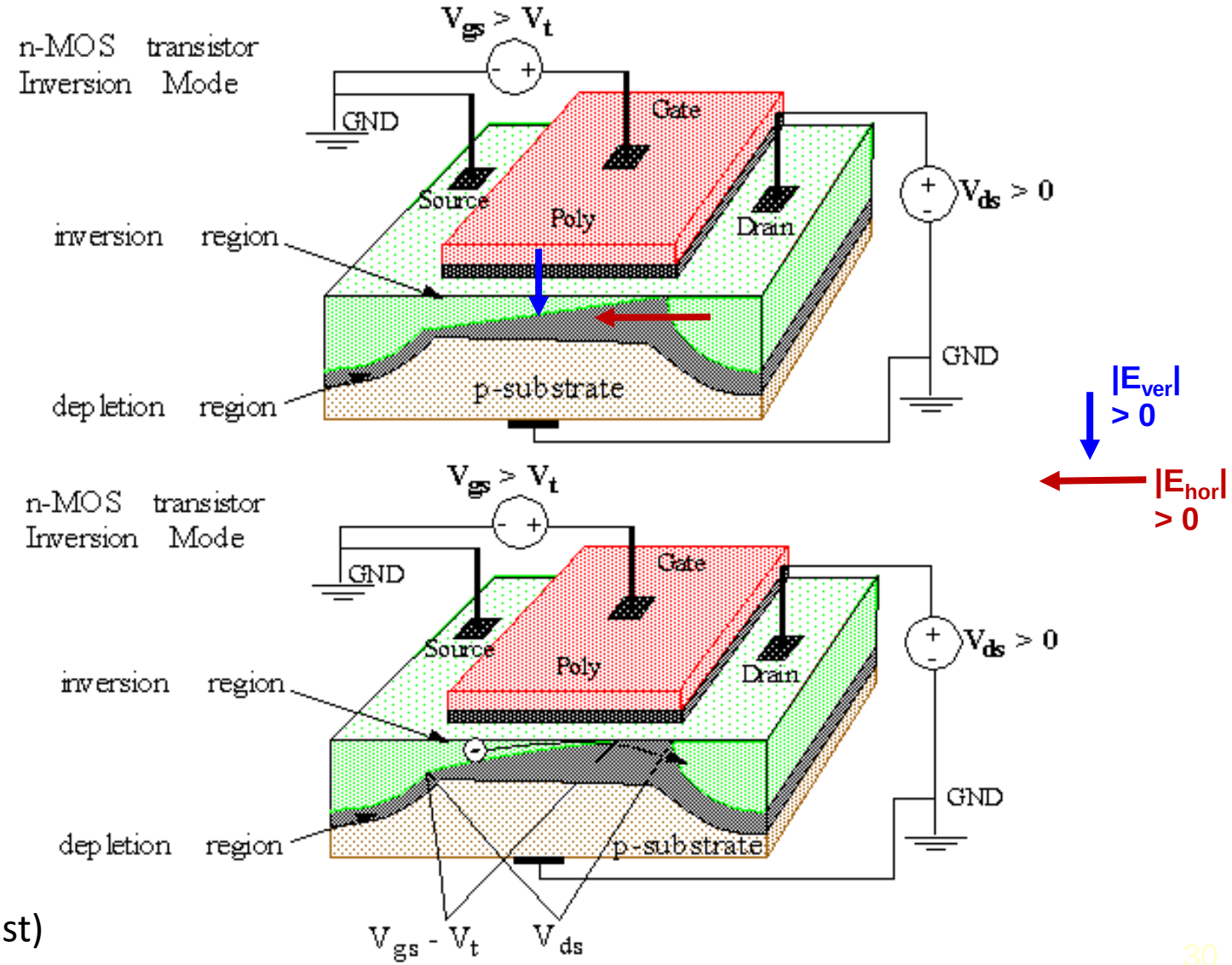
NMOS – Saturation

In **linear** region:

Vgs > Vt
and
0 < Vds < Vgs-Vt
(Vds ↑ => Ids ↑)

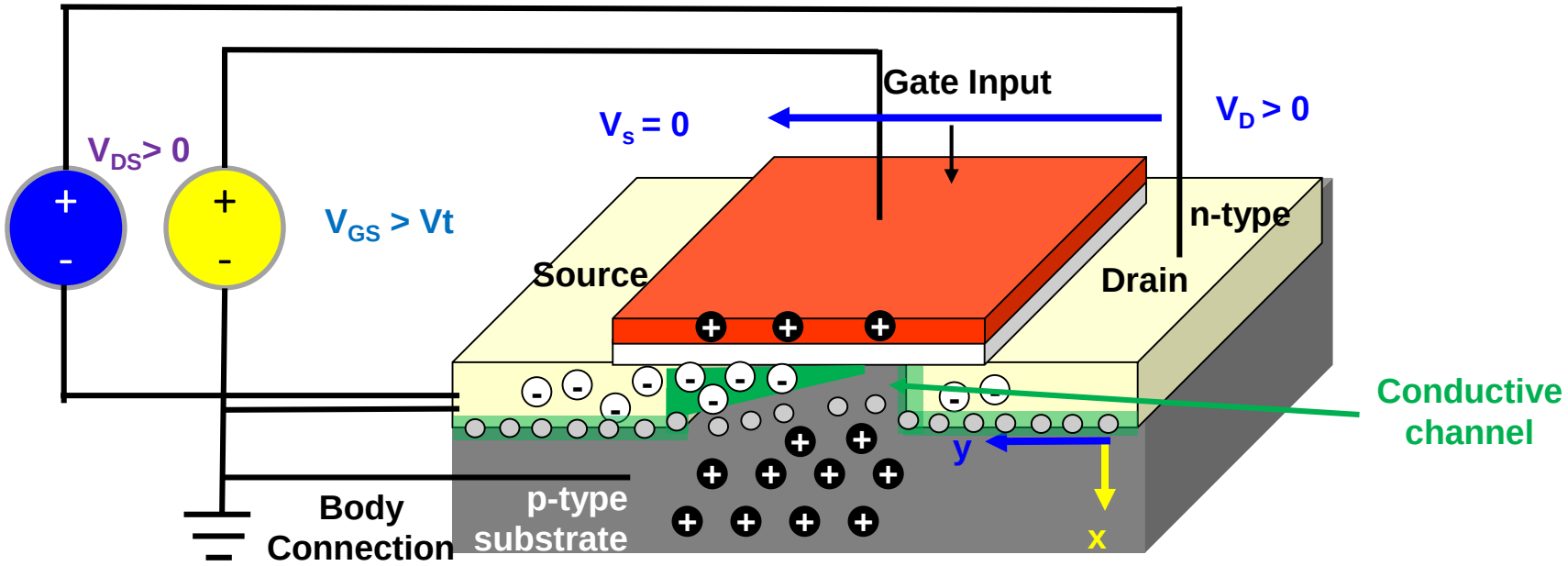
In **saturation** region:

Vgs > Vt
and
Vds > Vgs-Vt
(Vds ↑ => Ids = const)

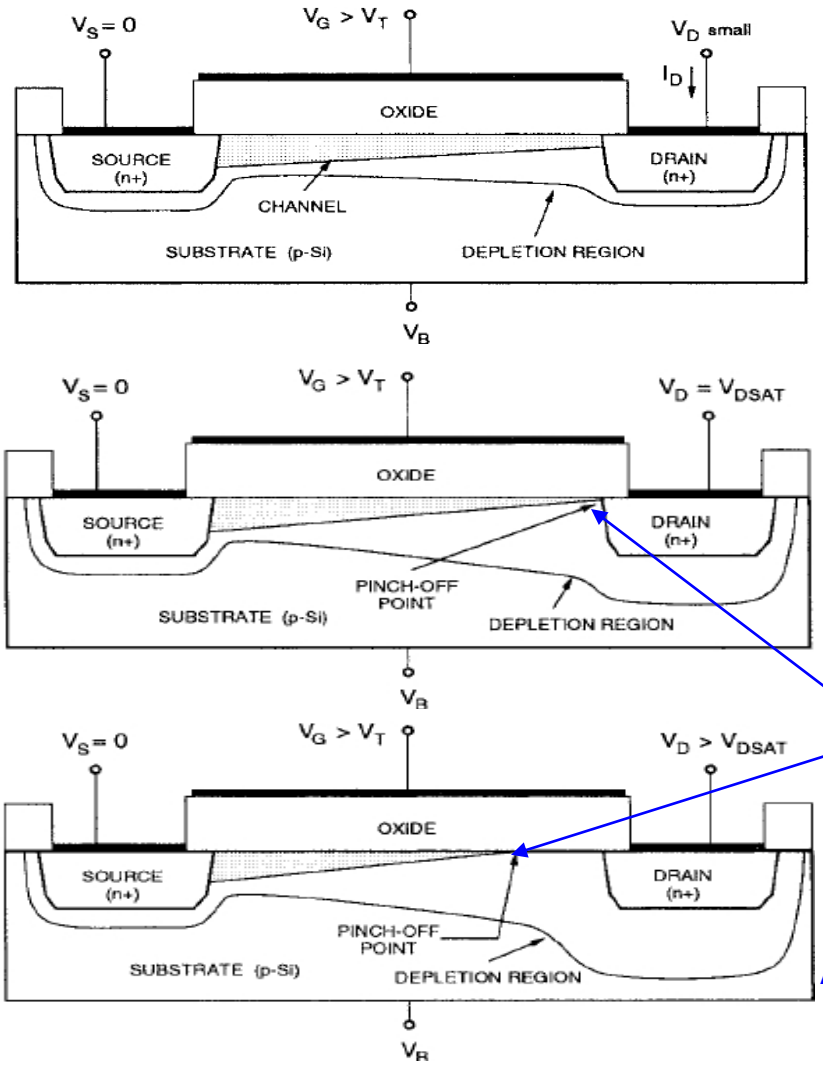


NMOS – Saturation

- Once $V_{DS} > (V_{GS}-V_T)$ the channel starts to pinch off
- At this point an increase in VDS (i.e. stronger electric field) doesn't induce more current
  - The extra energy being applied is used to simply get the electrons across the depletion zone between the pinched off channel and the drain
  - And as we increase VDS the channel pinches off even more meaning we have use more energy to get electrons across
  - Analogy: You can carry 15 items from one place to another in 10 minutes. I come to you and say, I'll give you a helper (increase VDS) but you have to transport 30 items (i.e. it becomes more work/harder). Does the rate of transfer change? No, your additional help/energy is wasted on the additional work you have to perform.



nMOS Cross-sectional View Summary



Operating in the linear region

Another way to think about it:
Vgs > Vgd so the channel is deeper near the source than the drain, but a continuous channel does exist

Operating at the edge of saturation

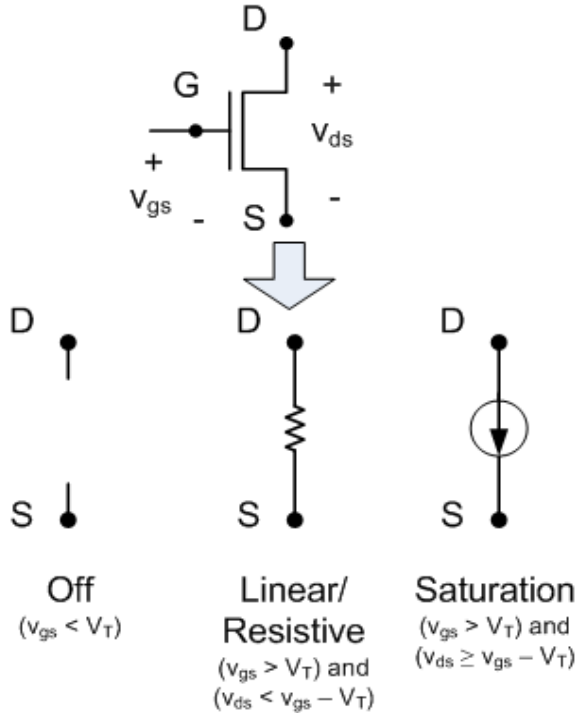
V_{DSAT} = Voltage where we crossed from linear (resistive) mode to saturation mode = Voltage at the pinchoff point =
This is the voltage at which electrons in the channel are pulled into the drain by Vds rather than staying at the surface due to Vgs

Operating beyond saturation

Any increase in V_D beyond V_{DSAT} is dropped across the depletion region from drain to the pinchoff point causing the channel to experience the same voltage V_{DSAT} on one side and thus the same amount of current to flow through the channel

Summary of MOS Transistor Modes

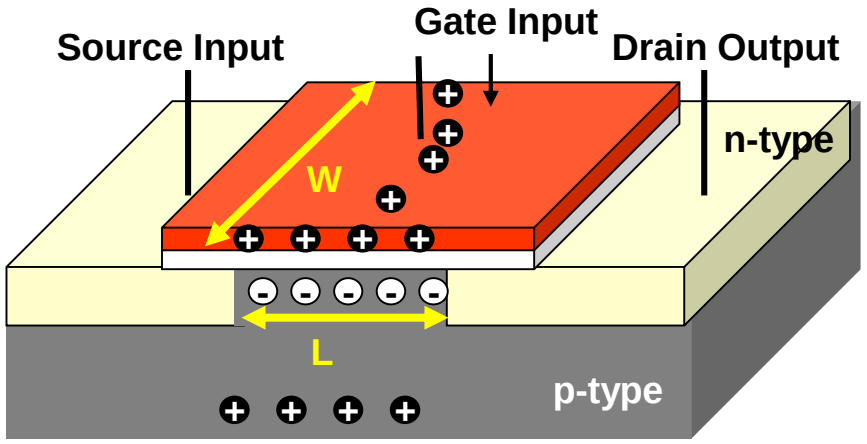
- MOS transistor (Ids/Vds relationship) can be modeled differently based on different operating conditions
  - Open circuit (off)
  - As a simple resistor between Drain & Source
  - As a constant current source between Drain & Source
  - Note: $K_n = \frac{\varepsilon_{ox}}{t_{ox}}\mu_n$ (K' = K_N for nmos, K_P for pmos)



Mode	Condition	Ids, Vds Relationship
Off	$v_{gs} < V_T$	$I_{ds} = 0$
Resistive	$v_{gs} > V_T$ and $v_{ds} < v_{gs} - V_T$	$I_{ds} = \frac{1}{2}K'\left(\frac{W}{L}\right)\left[2(v_{gs} - V_T)V_{ds} - {V_{ds}}^2\right]$
Saturation	$v_{gs} > V_T$ and $v_{ds} \geq v_{gs} - V_T$	$I_{ds} = \frac{1}{2}K'\left(\frac{W}{L}\right)\left[(v_{gs} - V_T)^2\right]$

Getting More Current to Flow

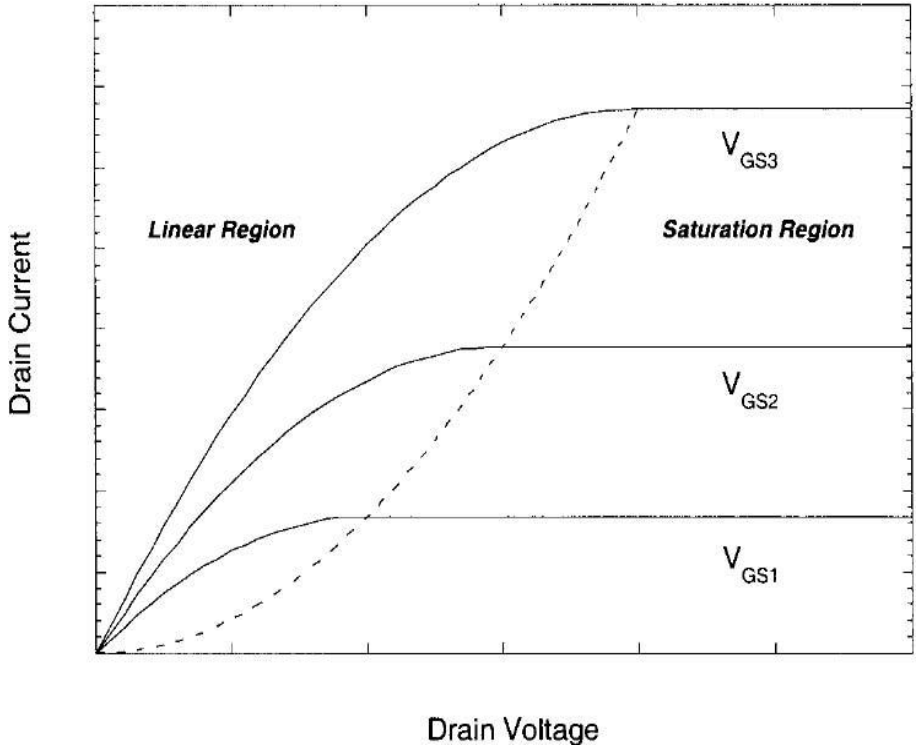
- Note: I_{ds} is proportional to K' (K_N or K_P) AND the ratio of W/L
- For a transistor $K_N = C_{ox}\mu_n = \frac{\varepsilon_{ox}}{t_{ox}}\mu_n$ is some **intrinsic** (**we can't change it**) measurement of how well the transistor we built will conduct…
  - [Note: $K_P = C_{ox}\mu_P \neq K_N$]
- As a designer we can change W and L
  - W ↑ = Conductivity ↑ ; L ↑ = Conductivity ↓
- As circuit designers, we can:
  - We can easily choose W & L
  - Hard to change K_N or K_P

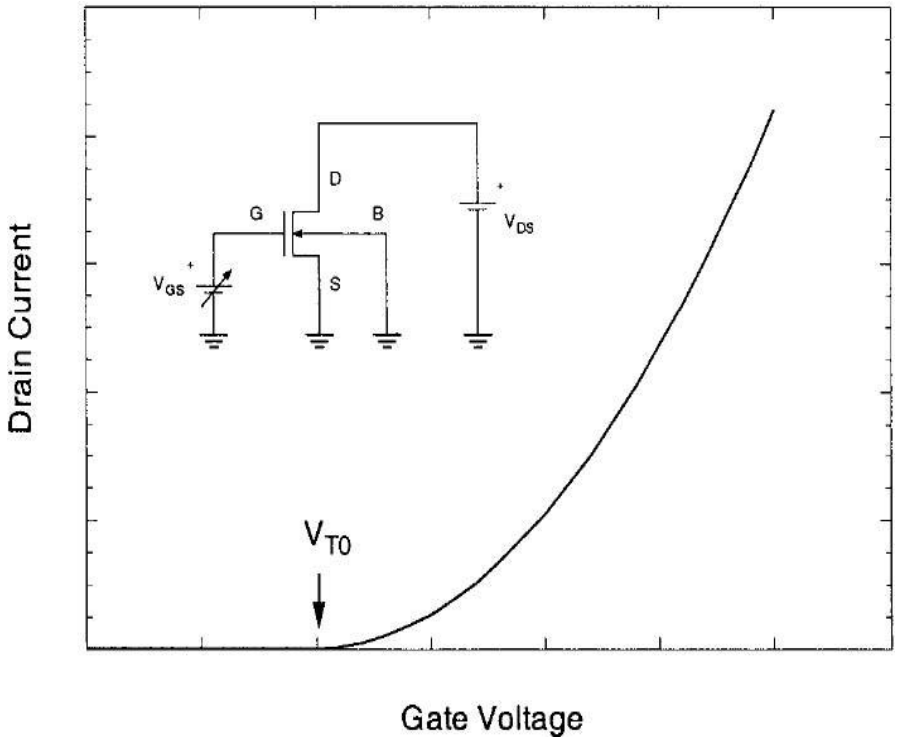


Changing W is something we will do a lot of in digital designs, mainly to influence delay of a gate

Mode	Condition	Ids, Vds Relationship
Resistive	$v_{gs} > V_T$ and $v_{ds} < v_{gs} - V_T$	$I_{ds} = \frac{1}{2}K'\left(\frac{W}{L}\right)\left[2(v_{gs} - V_T)V_{ds} - {V_{ds}}^2\right]$
Saturation	$v_{gs} > V_T$ and $v_{ds} \geq v_{gs} - V_T$	$I_{ds} = \frac{1}{2}K'\left(\frac{W}{L}\right)\left[(v_{gs} - V_T)^2\right]$

nMOS I_D as a Function of V_{DS} and V_{GS}

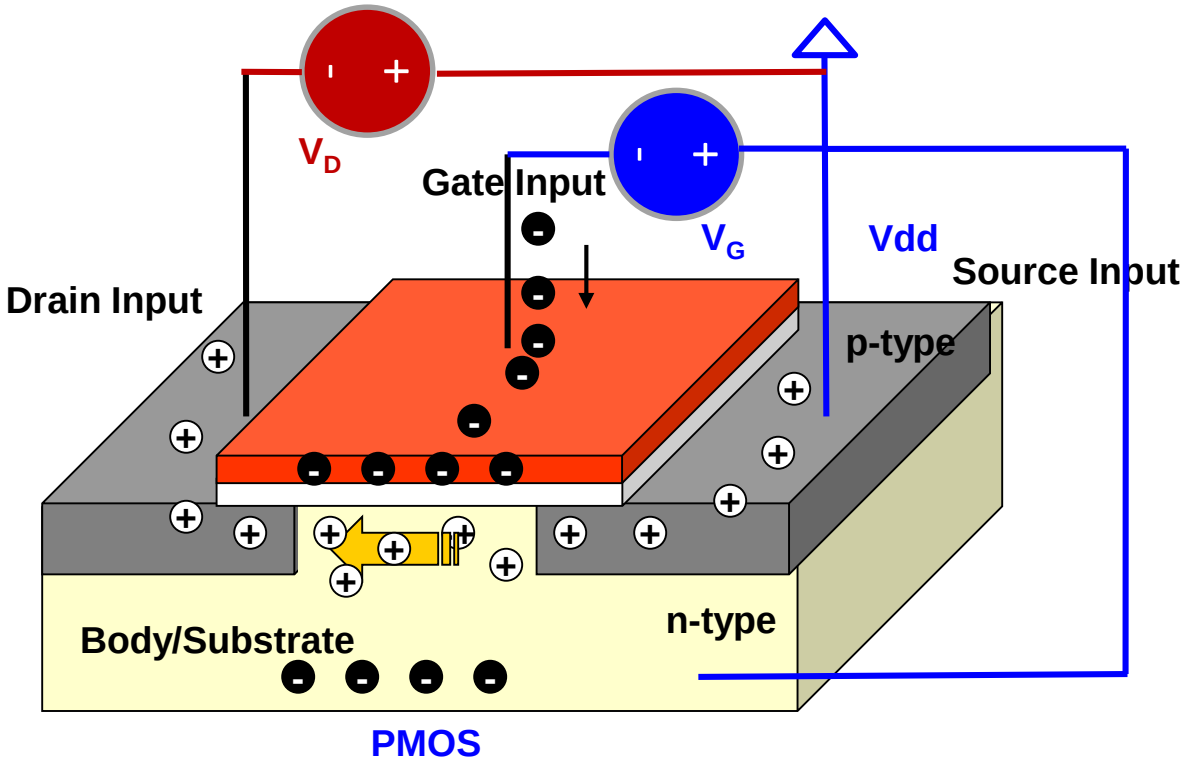




I_D vs V_{GS} for $V_{DS} > V_{DSAT}$

PMOS Operation

- Threshold voltage is now negative (e.g. -0.7V)
  - The gate has to be at a low enough voltage compared to the body to repel the electrons and attract free holes to create a conductive channel of holes



In cutoff:

$V_{gs} > V_t$

In linear region:

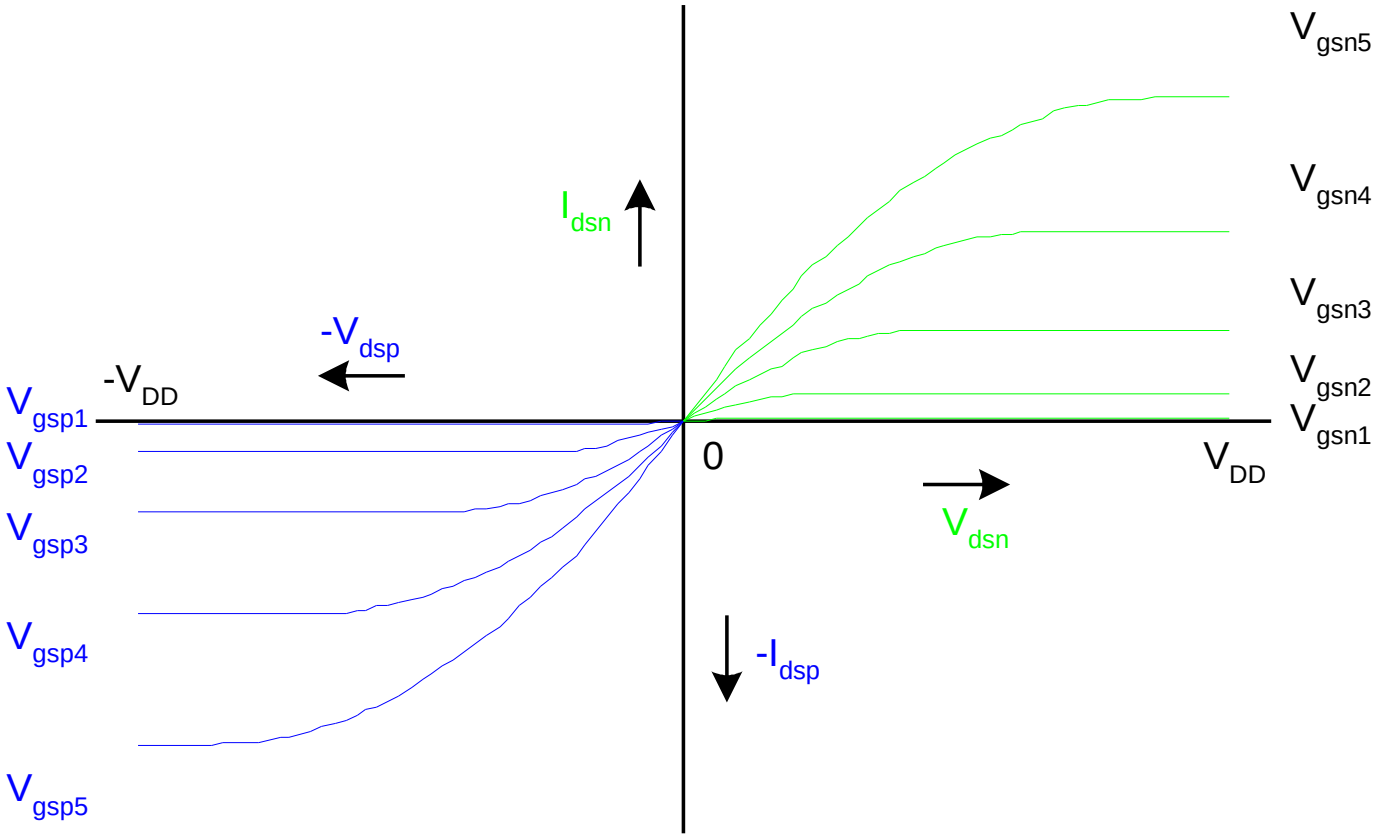
$V_{gs} \leq V_t$
and
$V_{gs}-V_t < V_{ds} < 0$

In saturation region:

$V_{gs} \leq V_t$
and
$V_{ds} < V_{gs}-V_t$

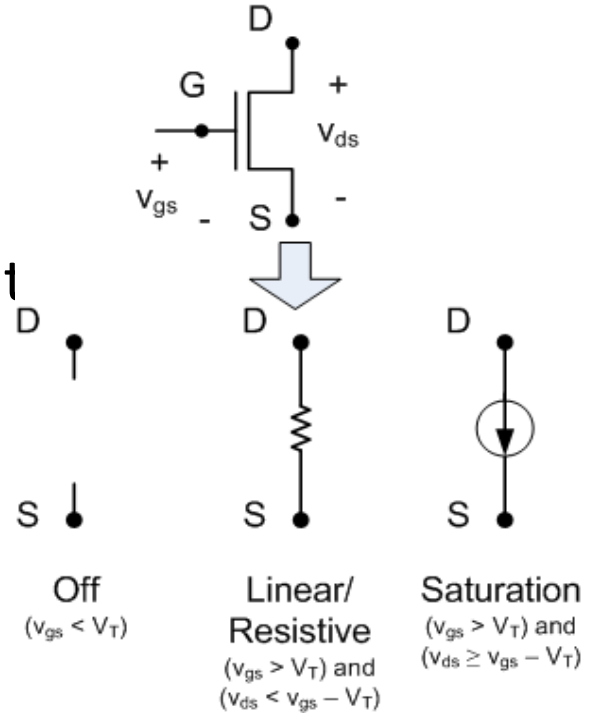
I-V Characteristics

- -Vdsp just means the drain is at a lower voltage than the source in the PMOS
- -Idsp just means the current is actually flowing from source to drain in the PMOS



Summary of NMOS or PMOS Transistors

- So that we don't get too caught up in the negative signs of PMOS transistors let us use the absolute value (ignore direction of current flow and sign of voltage) to arrive at one set of equations for either type
- We assume though:
  - NMOS: Vgs, Vt, Vds are all non-negative and current flows from D to S
  - PMOS: Vgs, Vt, Vds are all non-positive and current flows from S to D

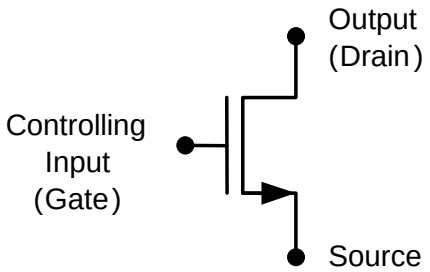


Mode	Condition	Ids, Vds Relationship
Off	$\|v_{gs}\| < \|V_T\|$	$\|I_{ds}\| = 0$
Resistive	$\|v_{gs}\| \geq \|V_T\|$ and $\|v_{ds}\| < \|v_{gs}\| - \|V_T\|$	$\|I_{ds}\| = \frac{1}{2}K'\left(\frac{W}{L}\right)\left[2(\|v_{gs}\| - \|V_T\|)\|V_{ds}\| - \|V_{ds}\|^2\right]$
Saturation	$\|v_{gs}\| \geq \|V_T\|$ and $\|v_{ds}\| \geq \|v_{gs}\| - \|V_T\|$	$\|I_{ds}\| = \frac{1}{2}K'\left(\frac{W}{L}\right)\left[(\|v_{gs}\| - \|V_T\|)^2\right]$

EXAMPLE DERIVATIONS

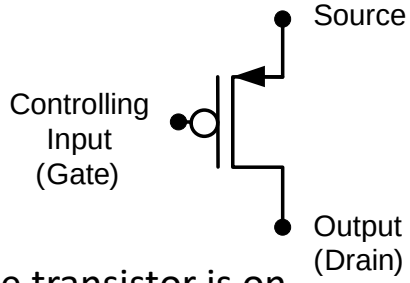
Example – NMOS Region Calculation

- V_t of an NMOS transistors is 0.35 v
- V_{DD} = 1.2v
- What are the conditions for the transistor to be
  - ON
    - $V_{GS} > 0.35$
    - Assuming Vs = GND, then Vg > 0.35
  - In Linear region
    - $V_{GS} > 0.35$ and $V_{DS} < V_{GS} - 0.35$
    - In a digital system Vg = 1.2V (logic 1) or 0V (logic 0) so assuming the transistor is on (Vg=1.2V), then $V_{DS} < 0.85$
  - In saturation region
    - $V_{GS} > 0.35$ and $V_{DS} >= V_{GS} - 0.35$
    - In a digital system, $V_{DS} >= 0.85$



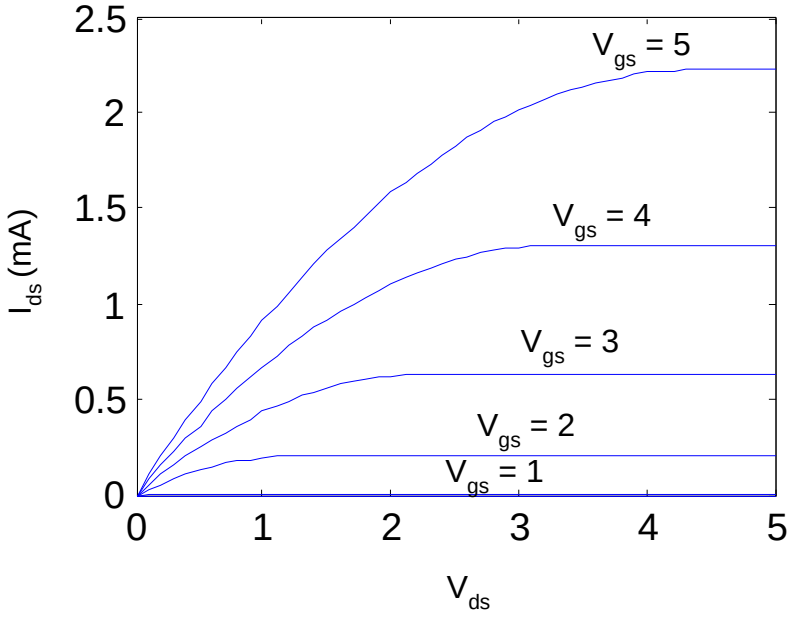
Example – PMOS Region Calculation

- V_t of a PMOS transistors is -0.35 v
- V_{DD} = 1.2v
- What are the conditions for the transistor to be
  - ON
    - $V_{GS} < -0.35$
    - Assuming Vs = Vdd = 1.2V, then Vg < 0.85V
  - In Linear region
    - $V_{GS} < -0.35$ and $V_{GS} - (-0.35) < V_{DS} < 0$
    - In a digital system Vg = 1.2V (logic 1) or 0V (logic 0) so assuming the transistor is on (Vg=0V), then $-0.85 < V_{DS} < 0$
  - In saturation region
    - $V_{GS} < -0.35$ and $V_{DS} < V_{GS} - (-0.35)$
    - In a digital system, $V_{DS} < -0.85$



Example – Current Calculation

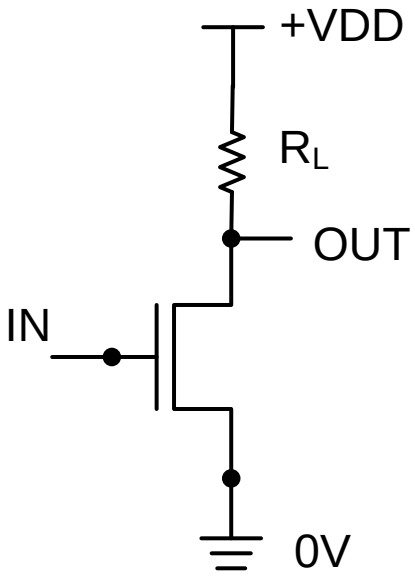
- A 0.6 μm process from AMI semiconductor
  - t_{ox} = 100 angstroms (1 angstrom = 1E-10 m = 1E-8 cm)
  - ε_{ox} =3.9*8.85E-14 F/cm
  - μ = 350 $cm^2/V.s$
  - V_t = 0.7 V
- Plot I_{ds} vs V_{ds}
  - V_{gs} = 0, 1, 2, 3, 4, 5
  - Use W/L = 4λ/2λ



$$\beta = \mu C_{ox}\frac{W}{L} = (350)\left(\frac{3.9 \bullet 8.85 \cdot 10^{-14}}{100 \cdot 10^{-8}}\right)\left(\frac{W}{L}\right) = 120\frac{W}{L}\mu A/V^2$$

Calculate Vout

- Given V_T = 0.5, V_{DD} = V_{GS} = 3V, K_N = 240 µA/V², W/L = 1, and R_L = 10KΩ
  - Note: Vout = V_{DS} and thus V_L = V_{DD}-V_{DS}
- Consider what mode the transistor is in, then setup a KCL equation at the output…
  - We know V_{GS}-V_T is 2.5 while VDS (=Vout) is very likely less-than 2.5 since we have a voltage divider and R_L = 10K with most of the 3V dropped across R_L leaving Vout to be small



$$I_{R_L} = I_{DS}$$

$$I_{R_L} = \frac{V_{DD} - V_{OUT}}{R_L} = \frac{1}{2} K_N \left(\frac{W}{L}\right) \left[2\left(|v_{gs}| - |V_T|\right)|V_{\text{OUT}}| - |V_{\text{OUT}}|^2\right]$$

$$\frac{3 - V_{OUT}}{10^4} = \frac{1}{2} 240 * 10^{-6}(1)[2(2.5)|V_{\text{OUT}}| - |V_{\text{OUT}}|^2]$$

Mode	Condition	Ids, Vds Relationship
Resistive	$\|v_{gs}\| \geq \|V_T\|$ and $\|v_{ds}\| < \|v_{gs}\| - \|V_T\|$	$\|I_{ds}\| = \frac{1}{2} K' \left(\frac{W}{L}\right) \left[2\left(\|v_{gs}\| - \|V_T\|\right)\|V_{ds}\| - \|V_{ds}\|^2\right]$
Saturation	$\|v_{gs}\| \geq \|V_T\|$ and $\|v_{ds}\| \geq \|v_{gs}\| - \|V_T\|$	$\|I_{ds}\| = \frac{1}{2} K' \left(\frac{W}{L}\right) \left[\left(\|v_{gs}\| - \|V_T\|\right)^2\right]$

Calculate Vout

- Given $V_T = 0.5$, $V_{DD} = V_{GS} = 3V$, $K_N = 240\ \mu A/V^2$, W/L = 1, and $R_L = 10K\Omega$
  - Note: Vout = V_{DS} and thus $V_L = V_{DD}-V_{DS}$

$$\frac{3 - V_{OUT}}{10^4} = \frac{1}{2} 240 * 10^{-6} \left(\frac{W}{L}\right) [2(2.5)|V_{\mathrm{OUT}}| - |V_{\mathrm{OUT}}|^2]$$

$$0 = -3 + V_{OUT} + 120 * 10^{-2} * \left(\frac{W}{L}\right) [5|V_{\mathrm{OUT}}| - |V_{\mathrm{OUT}}|^2]$$

$$0 = -3 + V_{OUT} + 6 * \left(\frac{W}{L}\right) V_{\mathrm{OUT}} - 1.2 * \left(\frac{W}{L}\right) * |V_{\mathrm{OUT}}|^2$$

- For W/L = 1:

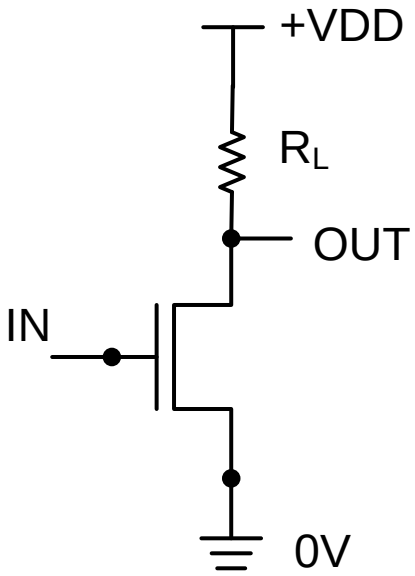
$$0 = -3 + 7 * V_{OUT} - 1.2 * |V_{\mathrm{OUT}}|^2$$

$$V_{OUT} = 0.46\ or\ 5.36$$

- For W/L = 2:

$$0 = -3 + 13 * V_{OUT} - 2.4 * |V_{\mathrm{OUT}}|^2$$

$$V_{OUT} = 0.24\ or\ 5.17$$

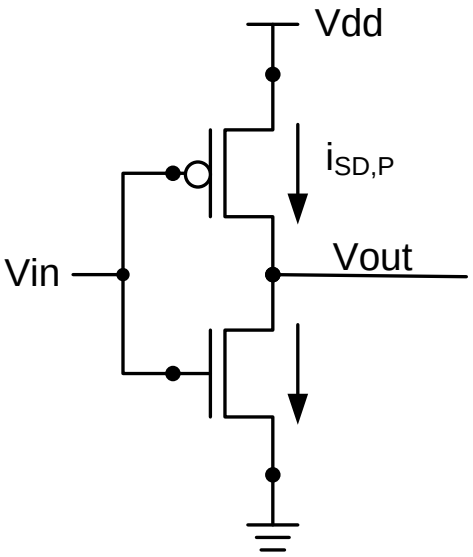


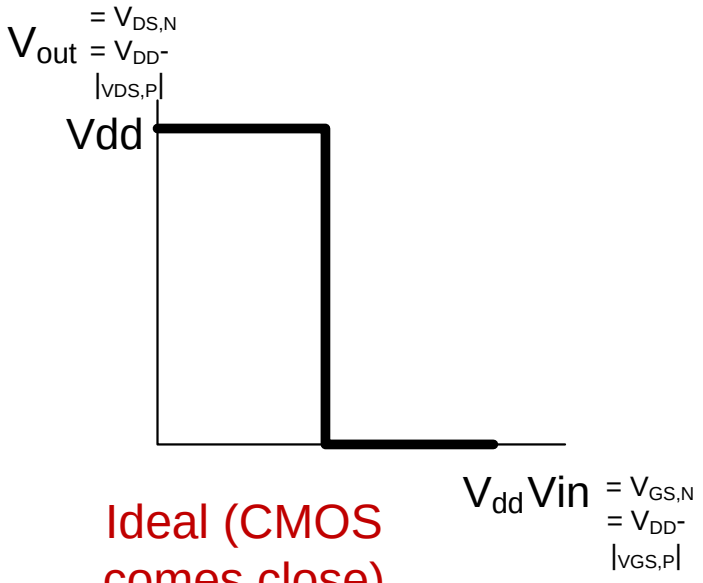
Calculating "DC" (Constant) Voltage Input/Output Relationship

STATIC INVERTER ANALYSIS

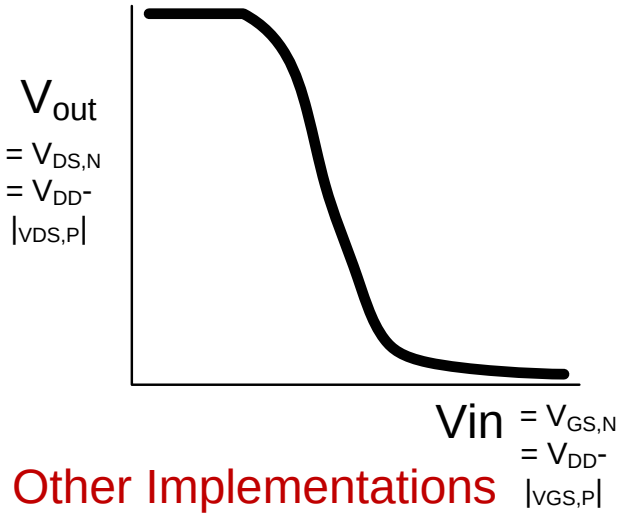
Recall the Inverter

- General problem: Given Vin and other parameters calculate Vout
- Take a moment and think: What should the plot of Vin vs. Vout look like
- How can we calculate Vout, given Vin?





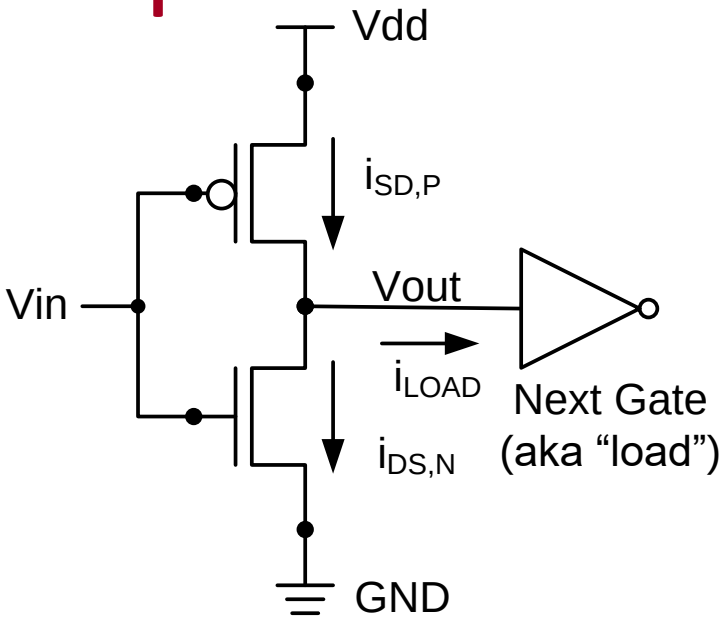
Ideal (CMOS comes close)

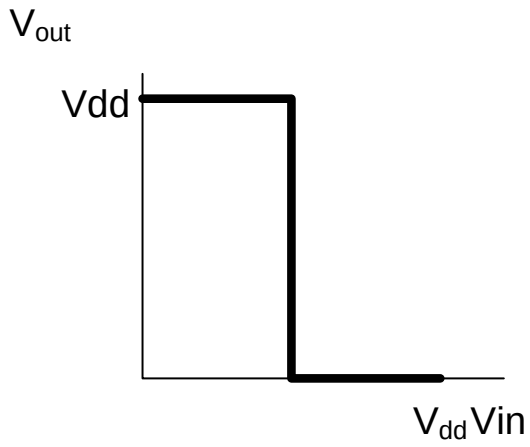


Other Implementations may be non-ideal

Step 1: Setup a KCL Equation

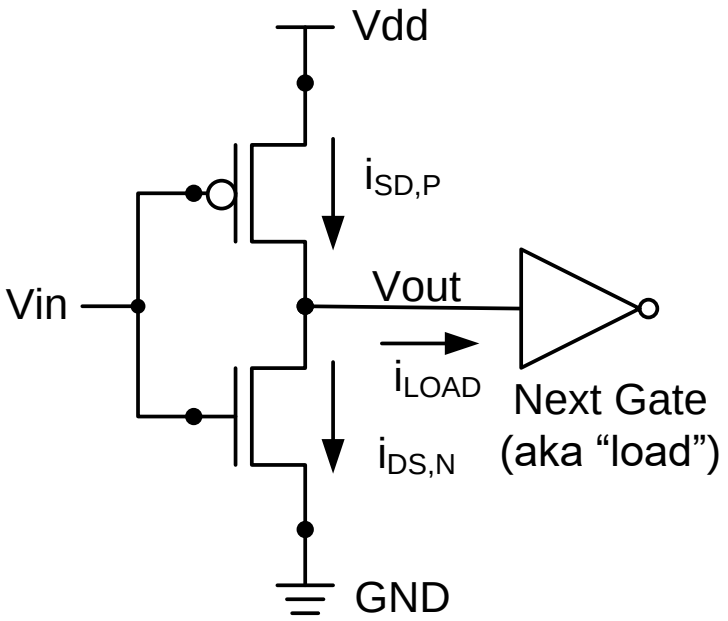
- Calculating the static ('steady state') Vin/Vout relationship?
- Use equations for MOS transistors by recognizing the following:
  - **$I_{SD,P} = I_{DS,N} + I_{LOAD}$ according to KCL**
  - $I_{LOAD} = 0$ (next gate = no current flow)
  - So **$I_{SD,P} = I_{DS,N}$**
    - The current through the PMOS must equal the current through the NMOS (we can set them equal) and we have equations for the currents ($|I_{DS,P}|$ and $|I_{DS,N}|$)

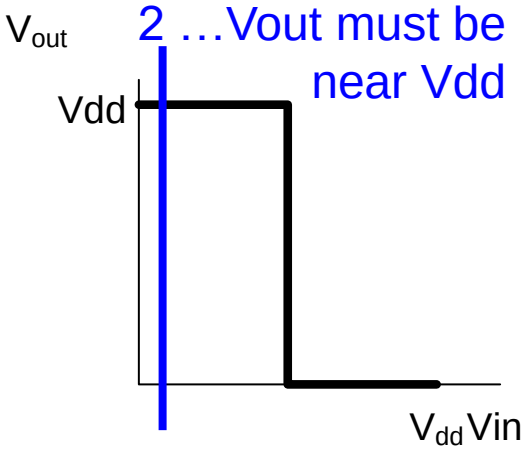




Step 2: Use Educated Guess for Modes of Operation

- But what mode are they in?
  - $V_{GS,N}$ = Vin – GND = Vin
  - $V_{DS,N}$ = Vout – GND = Vout
  - $V_{GS,P}$ = Vin – Vdd and $V_{DS,P}$ = Vdd – Vout
- Given the assumptions…
  - $V_{T,N} = V_{T,P}$ = 0.5V; Vdd = 3.0V; $k_n = 2k_p$; L=1; W_n = 1; W_p = 2; and Vin = 0.8V
- Then use the Vin/Vout relationship and the given value of Vin to make an educated guess
  - Since Vin is low, Vout should be "high-ish"
  - $V_{GS,N}$ – Vt = 0.3 and $V_{DS,N}$ = "high-ish"
    - NMOS is in SAT
  - $|V_{GS,P}|-|V_T|$ = 2.2-0.5 = 1.7V while $|V_{DS,P}|$ = 3V-"high-ish" = small (close to 0)
    - PMOS is in LINEAR





1. Because Vin = 0.8V…

Step 3: Setup Eqn & Solve for Vout

- Use the current equations for each transistor in its appropriate mode and solve for Vout

$$|I_{ds,p,LIN}| = \frac{1}{2}K_P{}'\left(\frac{W}{L}\right)_P\left[2(|v_{gs,p}| - |V_{T,p}|)|V_{ds,p}| - |V_{ds,p}|^2\right] =$$

$$|I_{ds,n,SAT}| = \frac{1}{2}K_N{}'\left(\frac{W}{L}\right)_N\left[(|v_{gs,n}| - |V_{T,n}|)^2\right]$$

$$\frac{1}{2}K_P{}'\left(\frac{W}{L}\right)_P\left[2(|v_{gs,p}| - |V_{T,p}|)|V_{ds,p}| - |V_{ds,p}|^2\right] = \frac{1}{2}K_N{}'\left(\frac{W}{L}\right)_N\left[(|v_{gs,n}| - |V_{T,n}|)^2\right]$$

$$\frac{1}{2}K_P{}'\left(\frac{2W}{L}\right)_N[2(|V_{dd} - v_{in}| - |0.5|)|V_{dd} - v_{out}| - |V_{dd} - v_{out}|^2] = \frac{1}{2}2K_P{}'\left(\frac{W}{L}\right)_N[(|v_{in}| - |0.5|)^2]$$

$$[2(|3 - 0.8| - |0.5|)|3 - v_{out}| - |3 - v_{out}|^2] = [(|0.8| - |0.5|)^2]$$

$$[3.4 * |3 - v_{out}| - |3 - v_{out}|^2] = 0.09$$

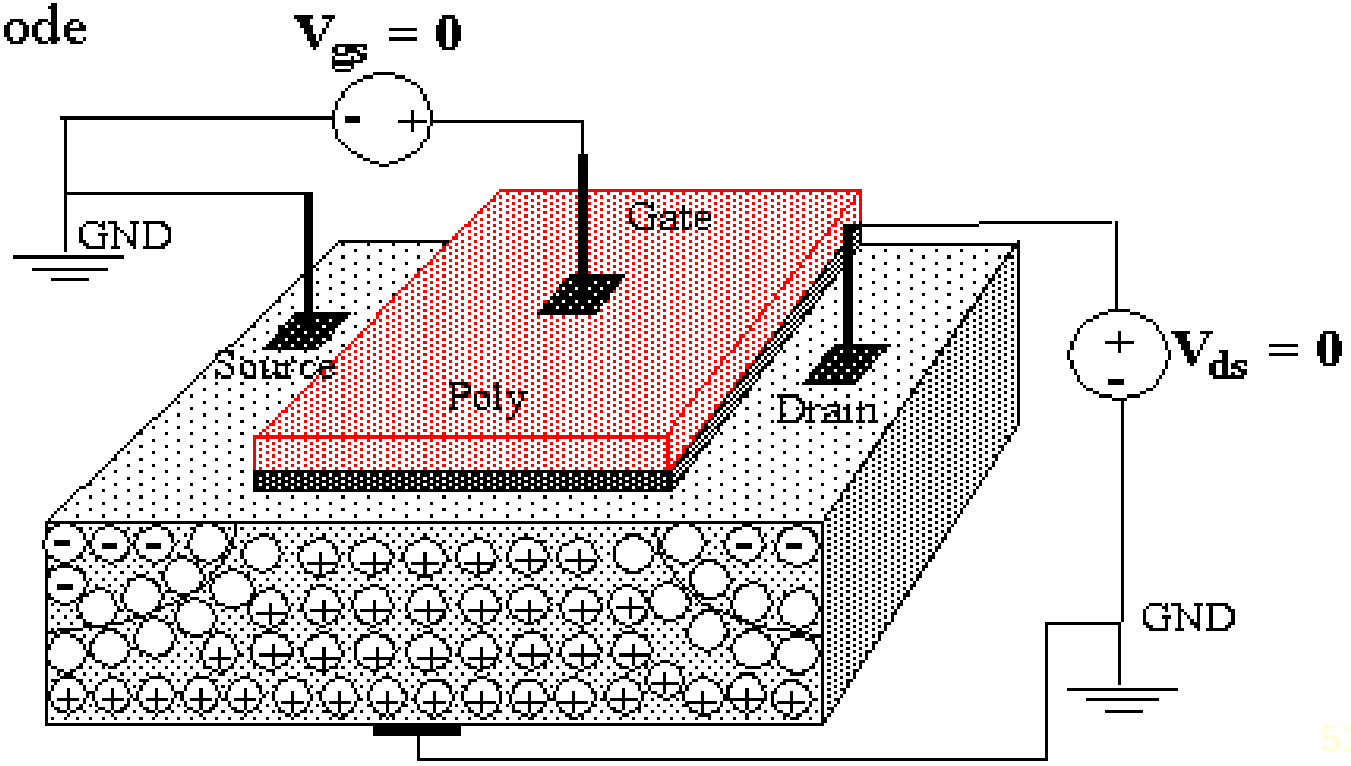
…continue on to solve for Vout

END LECTURE

NMOS – Accumulation

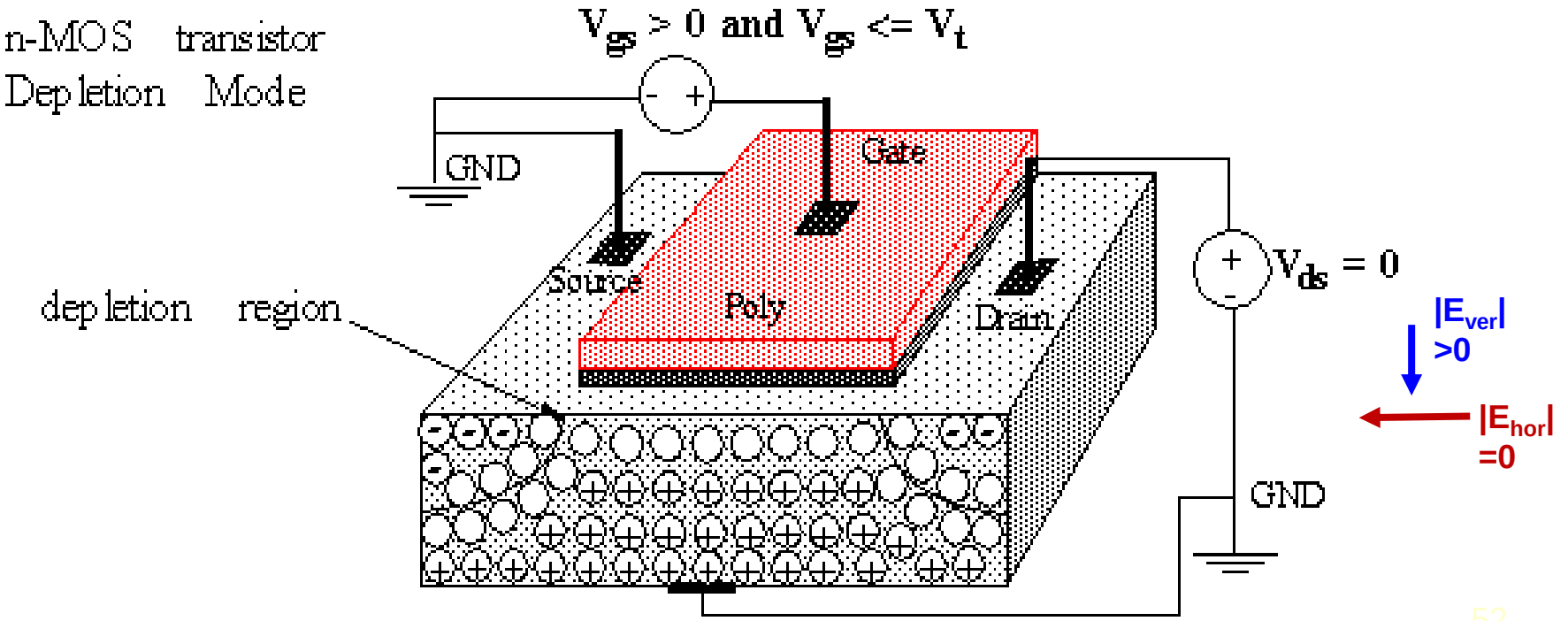
- Vgs ≤ 0
  - Actually attracts holes preventing a channel from forming

n-MOS transistor
Accumulation Mode



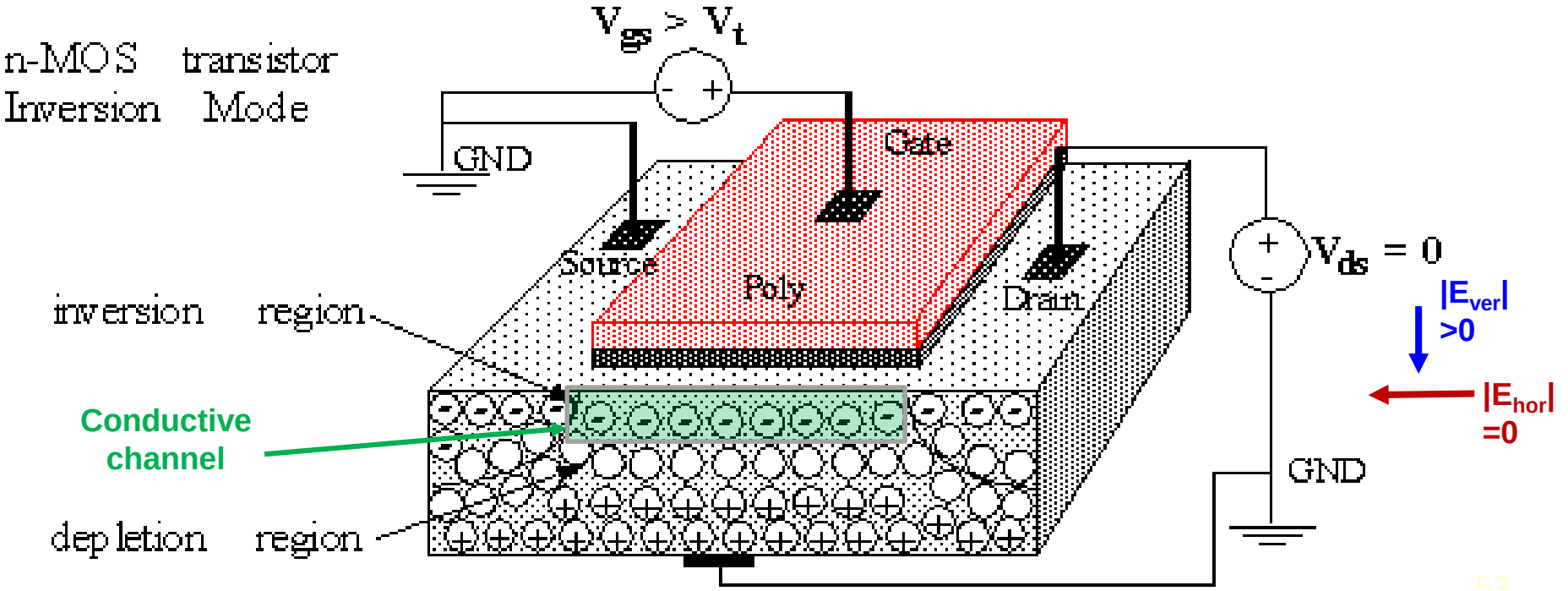
NMOS – Depletion

- For a small positive Vgs, positive holes are repelled creating a depletion region underneath the gate
  - The positive gate voltage is still not strong enough to attract enough free electrons (minority carrier in p-type body) to create a channel
  - Note Vds is still 0 (not electric field in the horizontal direction)



NMOS – Inversion

- For a Vgs > some threshold voltage (Vt) a conductive channel is created underneath the gate (the transistor is on)
  - Now Vgs is large enough to create the inversion layer (a.k.a. channel)



NMOS – Modes of Operations

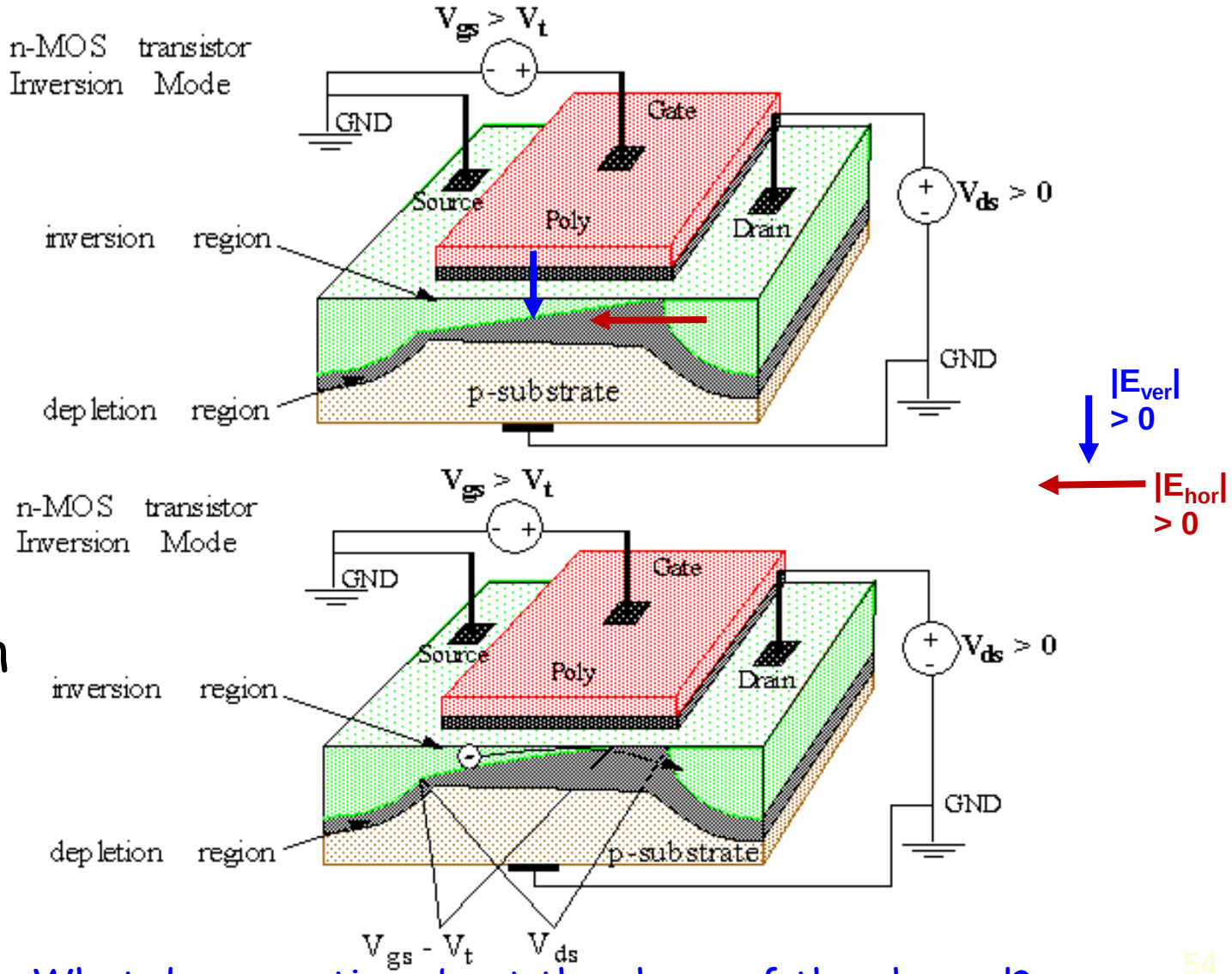
In linear region:

Vgs > Vt
and
0 < Vds < Vgs-Vt

Resistive mode
(Vds ↑ => Ids ↑)

In saturation region:

Vgs > Vt
and
Vds > Vgs-Vt
(Vds ↑ =>
Ids = const)



What do you notice about the shape of the channel?

Getting More Current to Flow

- Separate random fact: conductivity of material is $\sigma = q\mu n$ where μ=mobility and n is the concentration of free holes (or electrons depending on material type)
  - Note => Conductivity is 1/Resistance
  - These are intrinsic properties of the material and the level of doping
- For a transistor $K_N = C_{ox}\mu_n = \frac{\varepsilon_{ox}}{t_{ox}}\mu_n$ is some intrinsic measurement of how well the NMOS transistor structure that we built will conduct…
  - [Note: $K_P = C_{ox}\mu_P \neq K_N$]
- Note that W (Width of channel) and L (Length of channel) also effects conductivity…These are easy for us
  - W ↑ = Conductivity ↑ ; L ↑ = Conductivity ↓
- As circuit designers, we can:
  - We can easily choose W & L
  - Hard to change K_N or K_P
- You'll see us play with W & L a lot in digital designs, mainly to influence delay of a gate