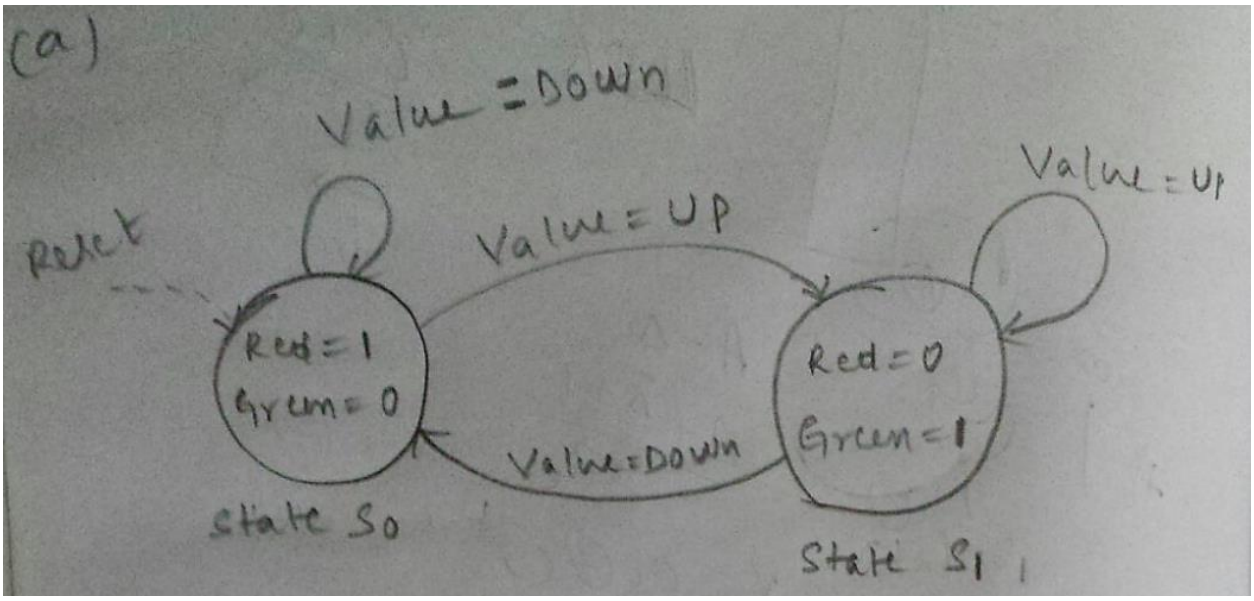
1.

a)

Let there are 2 states S0 and S1. State S0 correspond to state when the elevator is in ground and S1 correspond to state when elevator is in first floor




b)

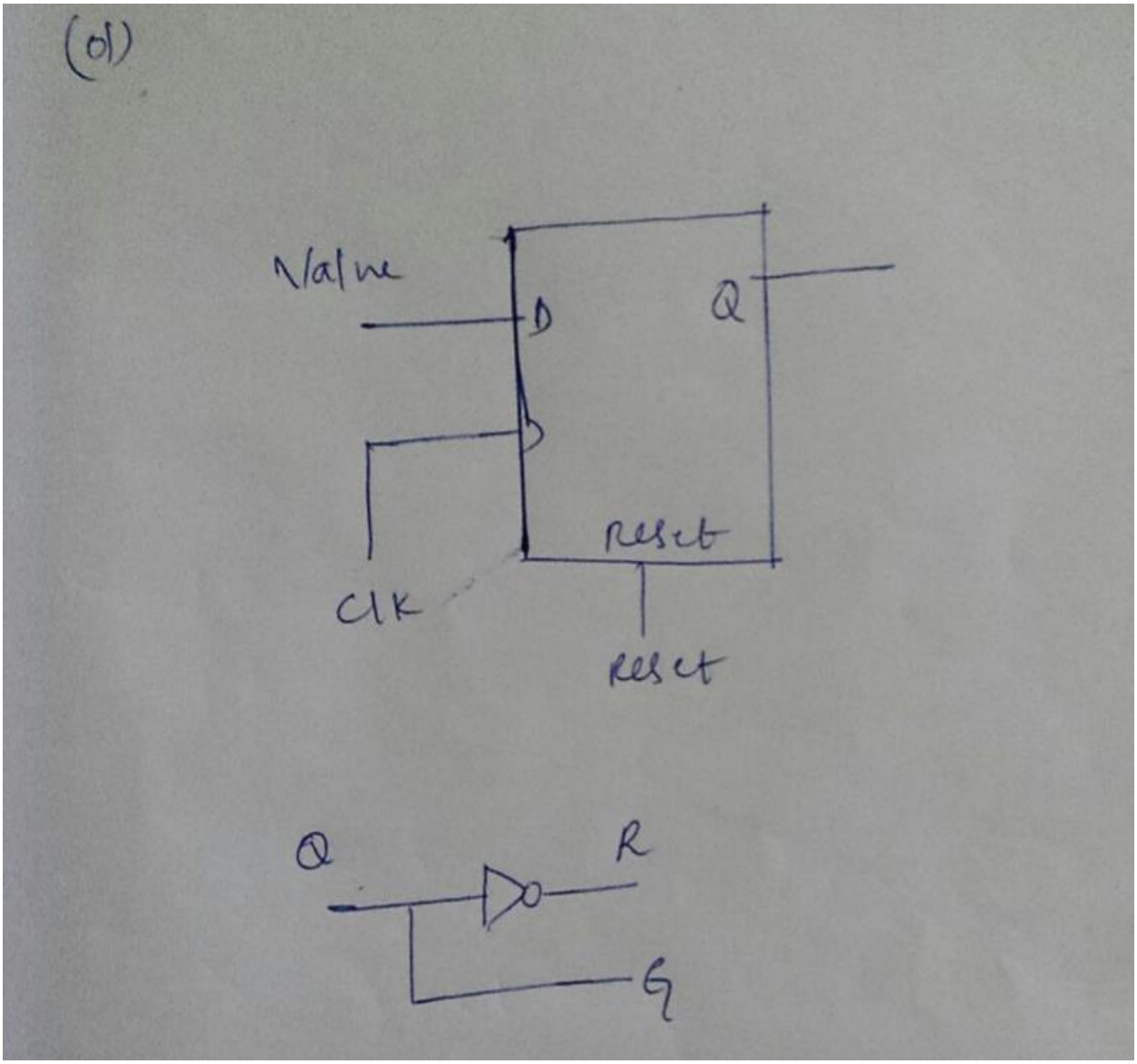
There are only 2 states. So One flipflop would be enough achieve the given task. Let's denote State S0=0 and State S1=1 where S0 correspond to state when the elevator is in ground and S1 correspond to state when elevator is in first floor. Also denoting Up=1 and Down=0 as values

| Present State(Q) | Present Input(Value) | Next State(Q*) | Output Green(G) | Output Red(R) |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 0 |

c)

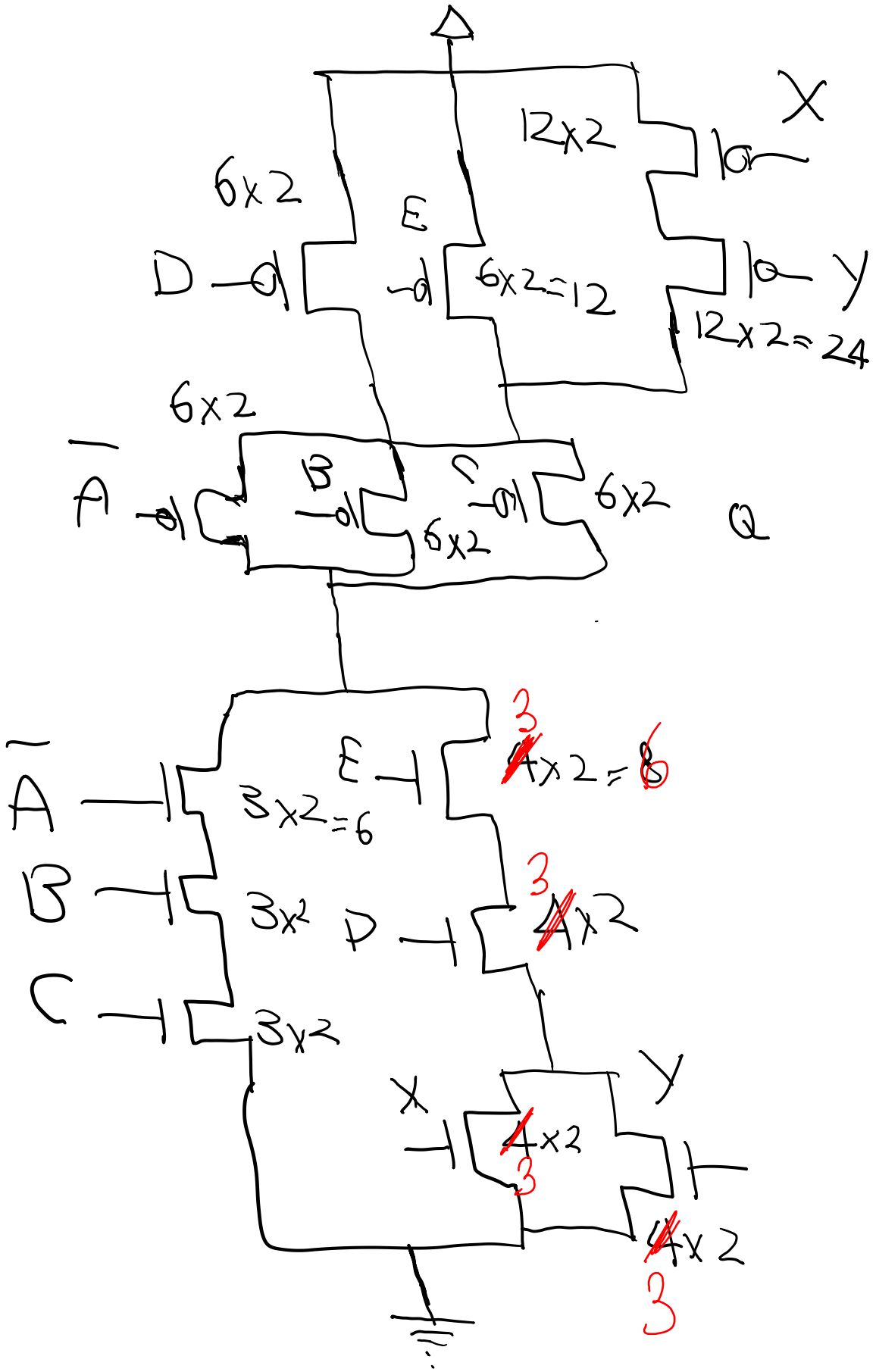
Q*=Value

G=Q and R=Q'




2.

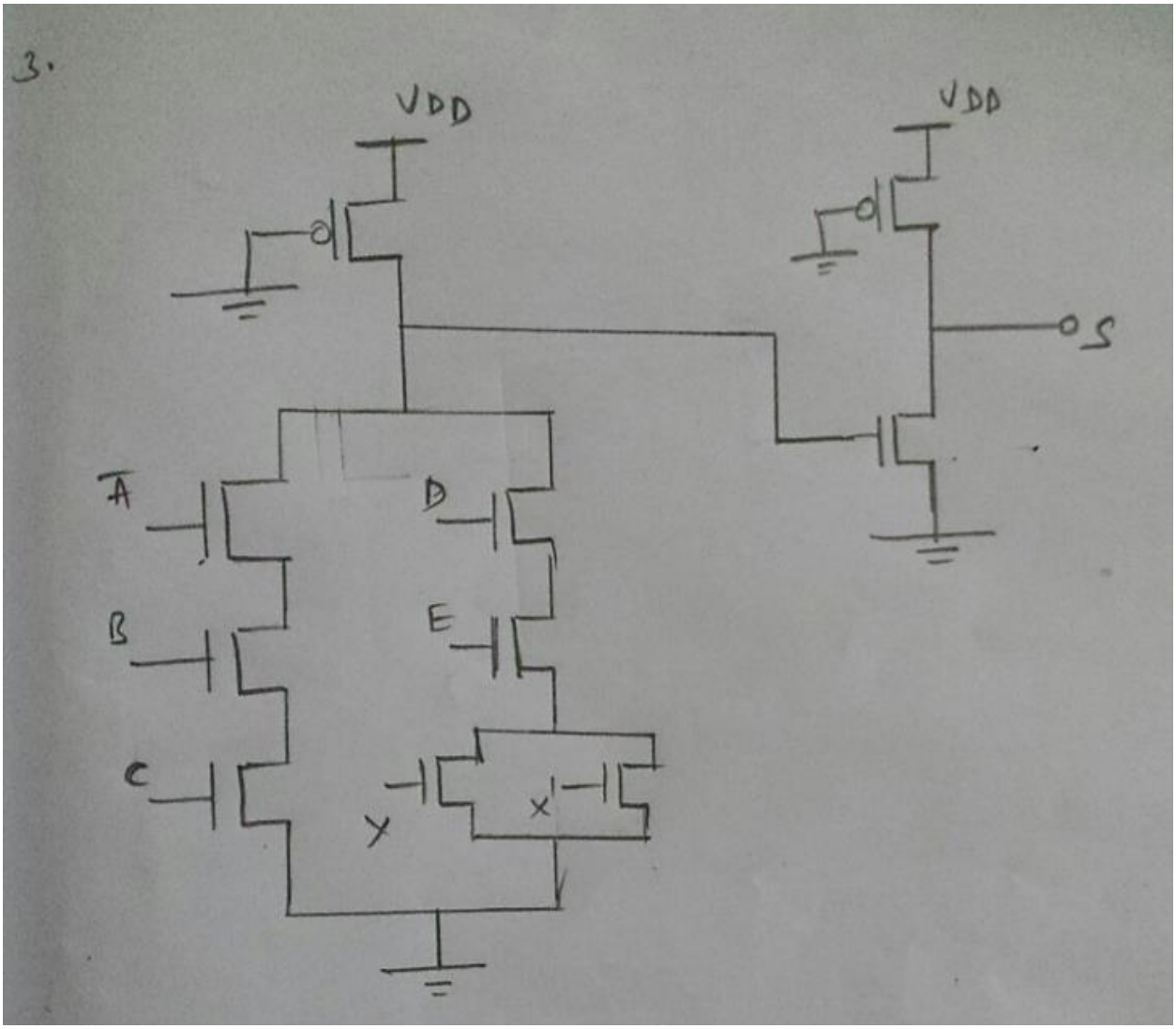
Mobility ratio=3, Also given that reference Inverter PDN(Pull down Network) has width of 2W and PUN(Pull up network) has width of 6W. It's clear that 6W/2W is also 3. This inverter is called 2X inverter. 1X inverter with 3W/1W also has mobility ratio of 3. We have doubled widths of all the transistors to get 2X inverter with same mobility ratio. Similarly for a given compound gate, we may do the sizing for 3/1 minimum then later choose to double it since reference inverter is 2X. Note that we may achieve the same by directly taking 6W/2W also. Therefore doubling (or multiplying by any X) the width of all the transistors will not change the mobility ratio.


X
12x2
6x2
E
D
6x2=12
Y
12x2=24
6x2
A
B
C
6x2
6x2
Q
3
E
4x2=8
A
3x2=6
B
3x2
3
D
4x2
C
3x2
X
Y
4x2
3
4x2
3

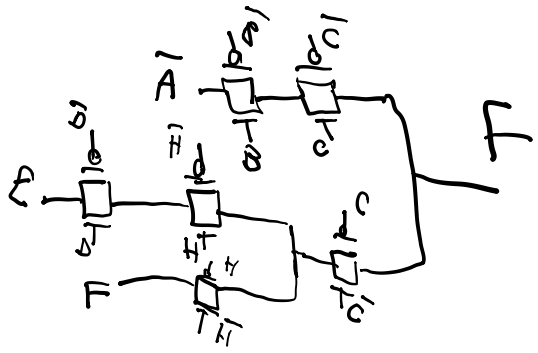
3.

This can be solved in 2 ways. By taking a double complement and then implementing as Pseudo nmos or by implementing it in stages.

3.



4.

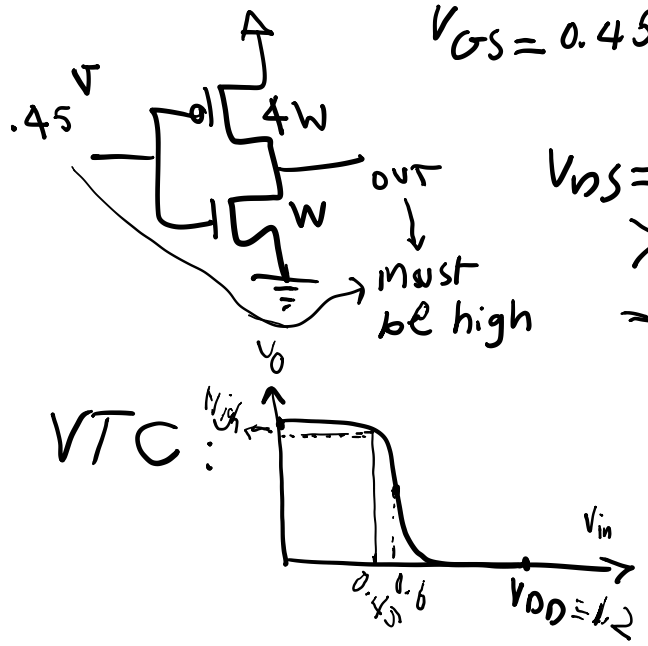


(b) To do the design using NMOS pass transistors only, we would remove all the PMOS transistors. Since all the transistors have the same size of W, then we would save half of the area:

TG-based area: 6*2*W

Pass-transistor-based: 6*W

5.




NMOS

$V_{GS}=0.45>.35$

$\Rightarrow$ ON

$V_{DS}=High-0$

$>0.45-0.35$

$\Rightarrow$ Sat.

PMOS

$V_{GS}=0.45-1.2$

$=-0.75$

$<V_{tp}=-0.35$

$\Rightarrow$ ON

$V_{DS}=High-1.2$

$>-0.75-V_{tp}$

$=-0.75+.35$

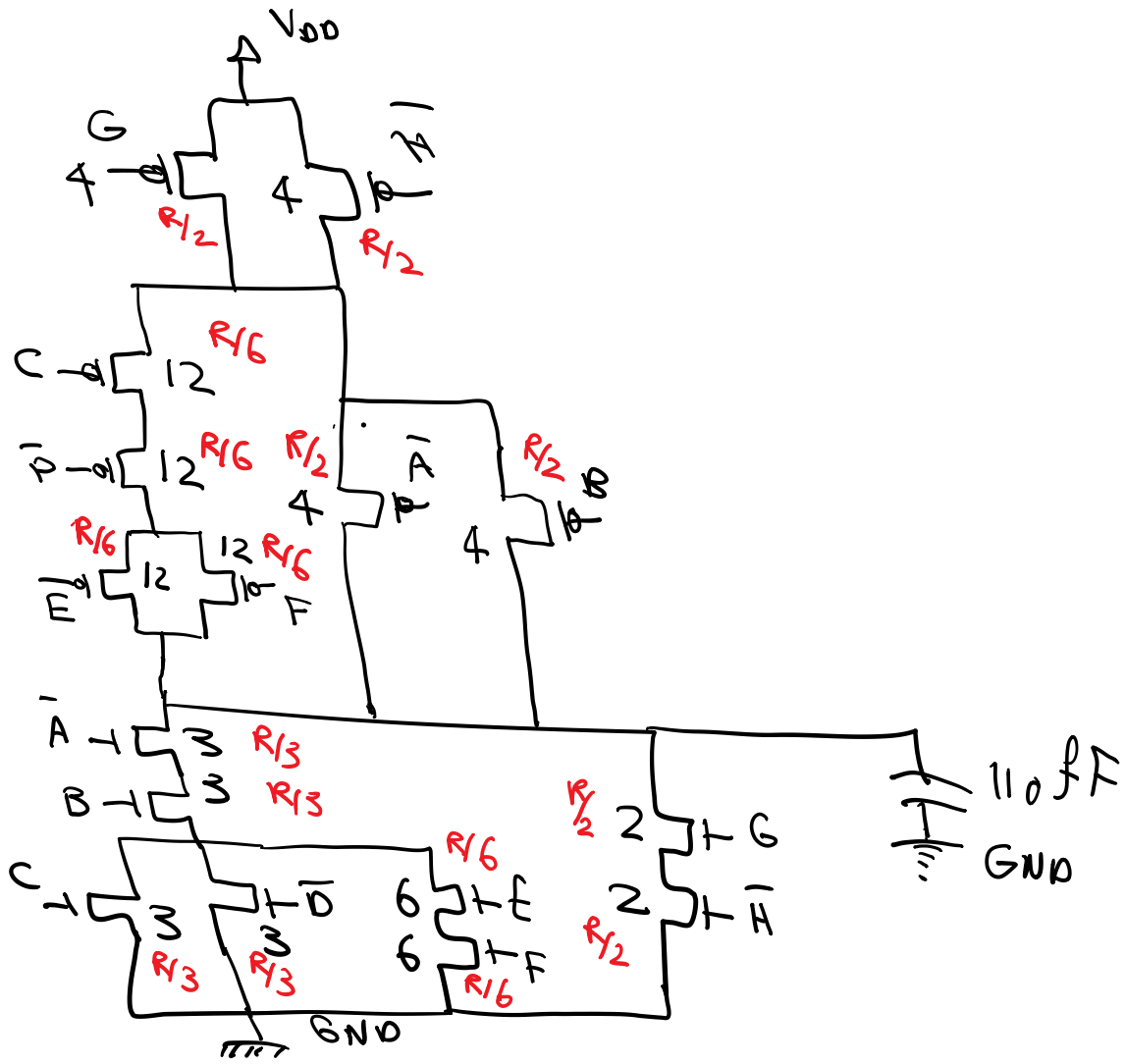
$=-0.4$

$\Rightarrow$ Lin.

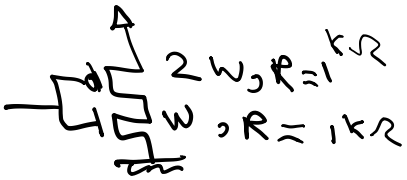
$$\frac{1}{2}\frac{k_n' W}{L_n}(V_{GS_n}-V_{tn})^2 = \frac{1}{2}k_p'\frac{4W}{L_p}\left(2(V_{GS_p}-V_{t_p})V_{DS_p}-V_{DS_p}^2\right)$$

$$\frac{k_n'}{L_n}(0.45-0.35)^2 = \frac{4k_p'}{L_p}\left(-0.8\times V_{DS_p}-V_{DS_p}^2\right)$$

6.




b) In the worst case only path is ON. However the way we have sized each path is to match the current drive of a reference Inverter, i.e., for each path the equivalent resistance is the same as the resistance of the reference Inverter:




Note: Please verify the above claim regarding the resistance of each path. As an example for the path involving E, D', C, and G in the PUN, the equivalent resistance is: R/6+R/6+R/6+R/2 = R. Another example: For the PDN path involving A', B, E, and F the equivalent resistance is: R/3+R/3+R/6+R/6=R

In the worst case the delay of our compound CMOS gate is 0.69RC = 0.69*1KOhms*110fF≈0.7*110*$10^{-12}$sec = 77psec

c) Time constant is RC = 1KOhms*110fF=110*$10^{-12}$sec = 110psec

d) Transition time is 2.2RC = 232psec

e) The main task is to figure out the equivalent resistance for the best case scenarios.

For rising: The equivalent resistance is $R_{equiv\text{-}rising\text{-}bestcase}$ = 5/32R = 5/32*10KOhms

For falling $R_{equiv\text{-}falling\text{-}bestcase}$ =7/16R = 7/16*10KOhms

Therefore in case of best case rising, the propagation delay, time constant and transition times are:

Propagation delay = 0.69* $R_{equiv\text{-}rising\text{-}bestcase}$ * 110fF

Time constant = $R_{equiv\text{-}rising\text{-}bestcase}$ * 110fF

Transition time = 2.2 * $R_{equiv\text{-}rising\text{-}bestcase}$ * 110fF

For best case falling:

Propagation delay = 0.69* $R_{equiv\text{-}falling\text{-}bestcase}$ * 110fF

Time constant = $R_{equiv\text{-}falling\text{-}bestcase}$ * 110fF

Transition time = 2.2 * $R_{equiv\text{-}falling\text{-}bestcase}$ * 110fF

7.

a. It's VDD – Vt = 0.7v
b. This is because the shortest channel means the highest possible current. This basically means utilizing the transistor up to its maximum current drive for the given width. W can then be used to increase the current even further, by widening the transistor, or lowering the current, by narrowing the transistor.
c. NOR: PUN has only one case, the worst case, cause the two transistors in series have to be ON to provide a pull-up current. However for the PDN, the best case is going to be twice as strong as the worst case, also twice as strong as the reference inverter, because both NMOS transistors are be ON.
   NAND: PDN has only one case, the worst case, cause the two transistors in series have to be ON to provide a pull-down current. However for the PUN, the best case is going to be twice as strong as the worst case, also twice as strong as the reference inverter, because both PMOS transistors are ON.
d. Looking at the transistor current equations and conditions, there are two ways: Either keeping the transistor in cutoff region (OFF) which means VGS should be less than Vt of the transistor for an NMOS and higher than Vt for a PMOS. Another option is to keep the transistors in the linear

region, but forcing Vds to be zero. E.g. for an NMOS that means VGS higher than Vtn but VDS less than VGS – Vtn. This for a PMOS means VGS should be less than Vtp and VDS higher than VGS - Vtp

e. Designing F in transistor level is time consuming, because we need to carefully size the transistor to get the optimal delay, noise margin, etc. However the benefit is that we could get the best design possible. Designing F in gate level needs an inverter, and AND gate and an OR. The benefit is that the design process is fast, because we could pick up the gates from the library and no transistor sizing is required. The downside is that the design may not be as efficient, in terms of area, speed, power consumption and noise robustness.