EE 209 Midterm II
Fall '15

Name: _____

Closed Book / 90 minutes **No CALCULATORS** **Score: _____ / 100**

Notes:

- If the test is long or difficult, do your best, we will curve/reduce the "perfect score"
- Assume all the inputs and their complements are available.
- Timing parameters using an RC model:

Voltage Range	Time
0 to 50% (t_p = prop. delay)	0.69*RC
0 to 63% (τ)	RC
10% to 90% (t_r=rise time/delay)	2.2*RC

- NMOS Transistor current in different operation regions:

Mode	Condition	Ids, Vds Relationship
Off	$v_{gs} < V_T$	$I_{ds} = 0$
Resistive	$v_{gs} > V_T$ and $v_{ds} < v_{gs} - V_T$	$I_{ds} = \frac{1}{2}K'\left(\frac{W}{L}\right)\left[2(v_{gs} - V_T)V_{ds} - {V_{ds}}^2\right]$
Saturation	$v_{gs} > V_T$ and $v_{ds} \geq v_{gs} - V_T$	$I_{ds} = \frac{1}{2}K'\left(\frac{W}{L}\right)\left[(v_{gs} - V_T)^2\right]$

1. **(20 pts.) FSM Design**

Design a controller for an elevator for two floors, Ground and First. There is one button that controls the elevator, and it has two values: Up or Down. Also, there are two lights in the elevator that indicate the current floor: Red for Ground, and Green for First. At each time step, the controller checks the current floor and current input, and properly changes floors and lights. Show the following:

a. The state diagram (Moore machine).
b. The transition table for the next state and the output.
c. Simplified the Boolean expressions for the next state and the output.
d. The gate level design.

2. **(15 pts.) CMOS Logic Design**
   Given Q = {A'BC+DE(Y+X)}'
   a. Design a CMOS compound cell that realizes Q. Show the schematic in transistor level.
   b. Size the transistors such that the design is as strong as a reference inverter with a PMOS and NMOS of sizes 6W and 2W, respectively. Assume the mobility ratio is 3.

3. **(10 pts.) Pseudo-NMOS Logic Design**
   Implement S = A'BC+DE(Y+X') in pseudo-NMOS.

4. **(15 pts.) Design Using Transmission Gates and Pass transistors.**
    a. Implement F = A'BC+C'(FH'+DEH) using transmission gates.
    b. For simplicity let us assume all the transistor sizes in part (a) are set to minimum width. How much area is saved if the design is converted to pass transistor type?

5. **(15 pts.) DC Analysis**

Set up a KCL equation to calculate the output voltage of a CMOS Inverter with sizes W and 4W (for the NMOS and PMOS, respectively) if the input is permanently connected to a low voltage value of 0.45V. Assume VDD=1.2v and $Vt_n = |Vt_p| = 0.35v$.

6. **(20 pts.) Transient Analysis**

A compound CMOS gate with output Y = {A'B(C+D'+EF) +GH'}' drives a load that has an effective capacitance of 110fF.

a. Size the transistors to match the current drive of a reference inverter with sizes W, and 2W.
b. Assume the equivalent resistance of each NMOS transistor with a size W, is 1KΩ. That for PMOS is 2KΩ. Find the worst case propagation delay of design.
c. Calculate the time constant.
d. Calculate the transition time.
e. Repeat parts (b) to (d) for the best case scenario.

7. **(5 pts.) Short Answer**
    a. VDD=1v, Vt_n = 0.3v. What is the highest voltage an NMOS transistor can pass?
    b. Briefly explain why all transistors in a design are typically fabricated with the shortest channel possible?
    c. A 2-input NOR gate and a 2-input NAND gate are sized to be equally strong and as strong as a reference inverter with sizes 4, and 1, in the worst case. How strong are they in the best case?
    d. How do you guarantee zero current for a transistor?
    e. What are the pros and cons of the following design methods to implement F = (AB' + C)'? 1) Design logic in transistor level, like what we did in the 2nd half of the semester, 2) Design logic in gate level like what we did in EE109 and first half of 209 semester.