EE 209 Homework 6
CMOS Gates

Name: ______________________________________

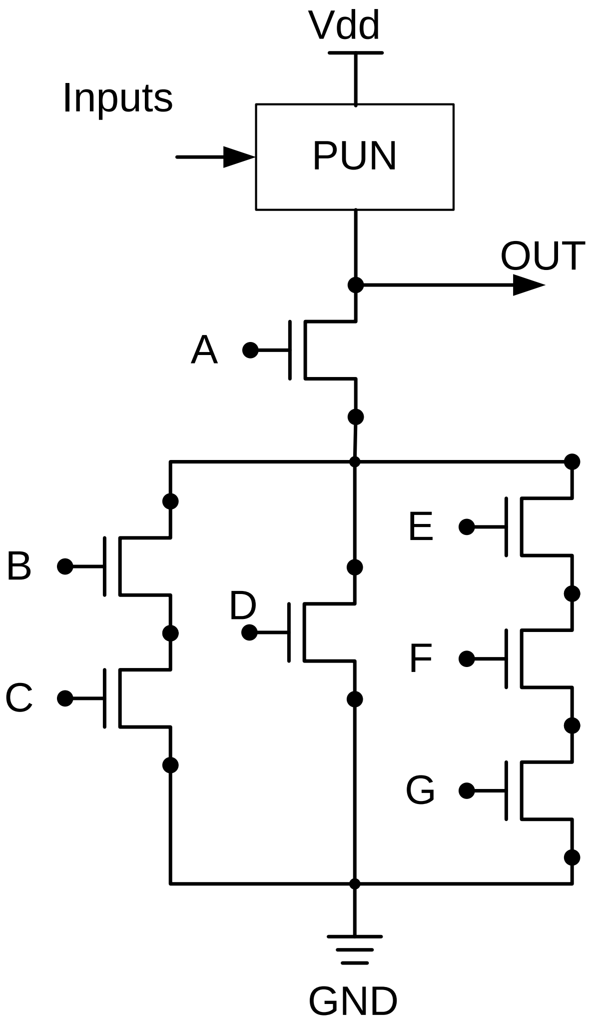
Due: See Website **Score:** ________

Paper Submission

[Helpful Videos to watch for your own knowledge]. Watch the following video clips on CMOS inverter fabrication and also the IC fabrication:

a. **CMOS Inverter fabrication: https://www.youtube.com/watch?v=OBiu2agne_U**
b. **An IC could have billions of transistors inside hundreds of millions of CMOS logic cells. The following video by Intel provides a very high level view of IC fabrication: https://www.youtube.com/watch?v=aCOyq4YzBtY**
c. **The following video is based on old technologies, however it still provides some useful information: https://www.youtube.com/watch?v=gBAKXvsaEiw**
d. **Interesting video on one application of PN junctions for solar cells. You can watch the video to see how solar energy can create electric power: https://www.youtube.com/watch?v=ZAxCvHxlLh8**

1. **Given the following pull-down for a CMOS compound gate.**
   a. **Draw the Pull-up network.**
   b. **Write the Boolean equation of OUT.**
   c. **Go back and show the widths of each NMOS and PMOS transistor such that the current in the worst case for rise time and fall time is equal to that of an inverter with minimum sized NMOS and equal rise and fall time.** $\frac{k_n}{k_p} = \mu_n/\mu_p = 4.$ **(μ refers to the conductance [ability to conduct current] of the given transistor type].**



2. CMOS and Sizing
    a. Draw the transistor level diagram of Y = (AB + CDE)' using a CMOS approach. Assume the complements (inverse) of each input is NOT available. Try to minimize the number of transistors used.
    b. Annotate your transistor schematic design from part a to show transistor widths (sizes) so that your implementation of Y matches the equivalent pull-up and pull-down resistance of a CMOS inverter. Assume the mobility ratio (i.e. μ_n / μ_p) is 2 and use minimum length transistors (L=1)
3. CMOS and Sizing
    a. Design a CMOS circuit that implements $G = [A'B + CD + E]$. Size the transistors such that the CMOS circuit is twice as strong (2x drive strength) as compared to a reference inverter with NMOS W=1 and PMOS W=3 size. (Assume inputs A, B, C, D and E as well as their complements are available)
4. NMOS-only and Resistive Loads
    a. Draw the schematic of Y = (ABG + CDEF)' using an NMOS-only approach (normal PDN using NMOS transistors but a single resistor in place of the PUN).
    b. Now, assuming that the input combination is such that the output *should* produce a logic '0' and that each NMOS transistor has a resistance of 5Kohm in linear mode, what value resistor would you be needed for the PUN to ensure Vout is at most 0.25*Vdd for the worst case input combination. Hint: Model the PDN as a single equivalent resistance value for the worst-case pathway when the PDN is ON so that you can use the voltage divider equation to relate Vout to Vdd, R_{PUN} and R_{PDN}.

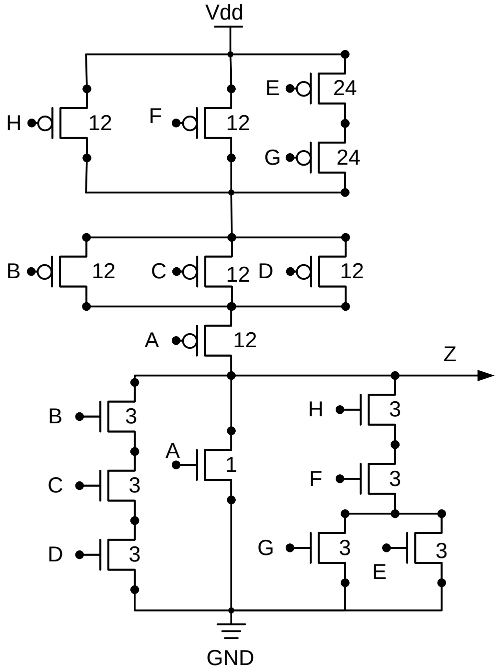
5. Use unit analysis to prove that the unit of RC is seconds

6. RC Transient Analysis: Given the equations for an RC circuit (i.e. for Vc(0)=0 we have $V_c(t) = V_{dd}\left[1 - e^{-\frac{t}{RC}}\right]$), verify the formula given below for the time constant, the propagation delay and the transition time (based on 10%VDD and 90%VDD crossing points) of the output voltage. To do this, simply set Vc(t) to the desired proportion of Vdd and solve for t. Show the details of your work.

Voltage Range	Time
0 to 63% (τ)	RC
0 to 50% (t_p = prop. delay)	0.69*RC
10% to 90% (t_r=rise time/delay)	2.2*RC

7. **Inverter Transient Analysis: The equivalent resistance values of a PMOS and an NMOS in an Inverter are 10KOhms and 7KOhms, respectively. The inverter drives an effective capacitance of 10fF (fF= femtoFarads = 10^{-15} Farads). Ignore other parasitic (internal) capacitances. Using an equivalent RC model to calculate the a.) propagation delay, b.) time constant and c.) transition time (based on 10%VDD and 90%VDD) for <u>BOTH</u> the rising output case and falling output cases (i.e. compute a., b., and c. for each of the rising and falling output cases).**

8. **CMOS Logic Design and Transient Analysis:**
   Below is the CMOS logic cell that outputs Z = ~(A+BCD+HF(E+G)). The transistors are sized assuming a mobility ratio of 4.
   a. **The equivalent resistance of an NMOS with a size of 1W is measured as 10KOhms and for a PMOS of size 1W is 40KOhms. The effective capacitance of the load is approximated as 100fF. Ignore other parasitic (internal) capacitances. Calculate the propagation delay (time for output to reach 0.5Vdd) of falling output in the <u>WORST CASE</u> scenario. Repeat for the rising output.**
   b. **Repeat your calculations to now find the <u>BEST CASE</u> propagation delay of the falling output and rising output**



9. **CMOS Inverter Static Analysis:**
   Setup a KCL equation to calculate the output voltage (Vout) of a CMOS inverter with sizes W and 2W (for the NMOS and PMOS, respectively) if the input is permanently connected to a high voltage of 2.4V. Assume VDD = 3.0V, Vtn = |Vtp| = 0.4V, $k_n=2k_p$. You need only setup the equation and manipulate it to be of the form $0 = aV_{out}^2 + bV_{out} + c$. Hint: Use an educated guess for the approximate level of V_{out} to determine the mode of operation of each transistor.