EE 209 Homework 5
Function Synthesis Techniques
and Sequential Building Blocks

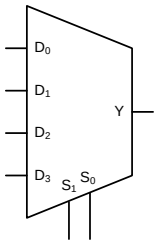
Name: _____

Due: See Blackboard

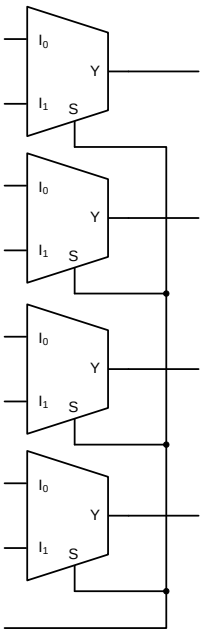
Score: _____

HW 5a Blackboard Form

1. **[BB] (12 pts.)** Apply Shannon's theorem to use only a 4-to-1 mux and inverters to implement the function **$F = \sum_{XYZ}(1,2,7)$.** Use the MSB's of the input as your select bits.



2. **[BB] (16 pts.)** Apply Shannon's Thoerem to build a circuit that takes two bits, X and Y, as input and produces 4 outputs: **X XOR Y, X < Y, X>Y and X==Y**. X < Y, X>Y and X==Y should be the comparison results of the single bits X and Y. To implement this circuit use four 2-to-1 muxes whose select bits are tied to a single input. Use X as your select bit. You may assume that both the complement and true form of the input variables are available (i.e. X and X' can be used as inputs). As always constant 0's and 1's can be connected to inputs. Clearly label the inputs and outputs to generate the indicated functions.



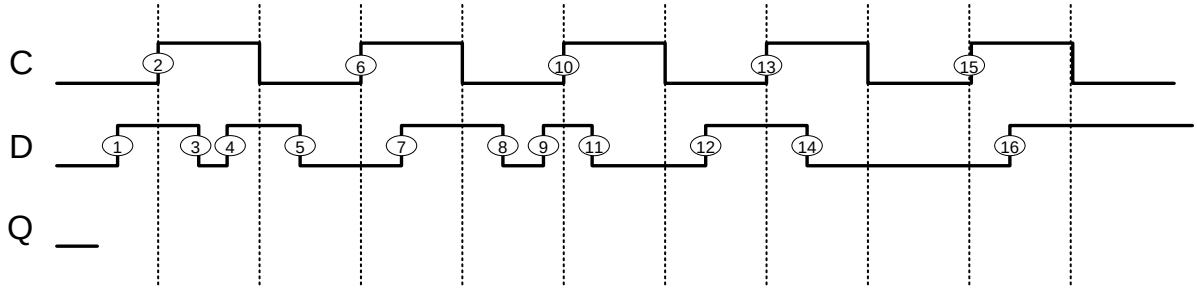
3. **[BB] (17 pts.)** Using Shannon's theorem, split the function Z shown below on the A variable to yield Z(0,B,C,D) and Z(1,B,C,D). Show how to implement the entire function Z using a 2-to-1 mux plus basic logic gates (AND, OR, etc.).

A	B	C	D	Z
0	0	0	0	**0**
0	0	0	1	**1**
0	0	1	0	**0**
0	0	1	1	**1**
0	1	0	0	**1**
0	1	0	1	**0**
0	1	1	0	**d**
0	1	1	1	**0**
1	0	0	0	**1**
1	0	0	1	**1**
1	0	1	0	**0**
1	0	1	1	**0**
1	1	0	0	**d**
1	1	0	1	**1**
1	1	1	0	**0**
1	1	1	1	**d**

4. **[BB] (18 pts.)** For each of the following functions list the size of ROM required to implement it (e.g. 256x4 or 8x1). Then, draw the block diagram of the ROM showing the device labels: A[n-1] to A[0] and your data outputs as D[m-1] to D[0] [device labels are inside the block used to indicate which input/output is which] label the address inputs]. Next add appropriate system labels (actual function input and output signals). You need not show the contents of the ROM, just the size.
   a. A circuit that converts a 3-bit 2's comp. number X[2:0] to the equivalent 4-bit signed magnitude number, Y[3:0].
   b. H = Π ABCD(2,5,6,7,8,10,13,15)
   c. A circuit that takes a 6-bit 2's comp. number, A[5:0], and squares it (B = A2) where B is output in unsigned representation (i.e. squaring always yields a positive result.)

HW 5b Blackboard Form

5. **[BB] (16 pts.)** Complete the following waveform for a D-Latch with active-high clock (Remember latches are level sensitive). To enter your answer online, select which transitions of the clock, C, or the D-input (indicated by a timestamp) will cause Q to toggle (i.e. change from 0 to 1 or 1 to 0). If Q doesn't change do not enter that timestamp as an answer.



6. **[BB] (21 pts.)** Complete the waveform for the following design involving two negative edge-triggered D flip-flops. Note: OUT is a combinational logic function of the FF outputs. Note: Combinational logic gates are UNAFFECTED by the clock (only FF's use the clock signal). Thus, a change in the inputs to logic gates causes an immediate change (after a small propagation delay) in the outputs. For D1 and D2 indicate their value during the middle of clock cycles A through F. For OUT indicate which timestamps of D or CLK will cause (either directly or via D1 and D2) OUT to toggle (from 0 to 1 or 1 to 0)