EE 209 Homework 4
Adders and Counters

Name: _____

Due: See Blackboard **Score: _____**

For Blackboard based questions, enter your answers in the submission form. For Xilinx based questions, you should upload a your Verilog design files (not the testbenches, just the design file related to that question) to Blackboard. We have provided testbenches so that you can simulate your design and mentally check the given output to what you would expect based on the problem description. This should ensure that your design is correct before you submit.

HW 4a Blackboard Form (16 pts.)

1) [BB] (16 pts.) Perform the following addition and subtraction problems assuming 2's complement numbers. State whether overflow does or does not occur for each problem. Justify your answer for why overflow does or does not occur. (You can easily check your work by converting to decimal.)

a.)
```
 1010 0110
+1101 1011
```

b.)
```
 0010 0001
+0111 1001
```

c.)
```
 1000 0010
-1010 1111
```

d.)
```
 0101 1001
-1010 0101
```

HW 4b (41 pts.) – Xilinx Submission – Upload your 3 Verilog design files related to these 3 questions to Blackboard HW4b assignment.

Remember first download the skeleton project and then complete the Verilog module for each question.

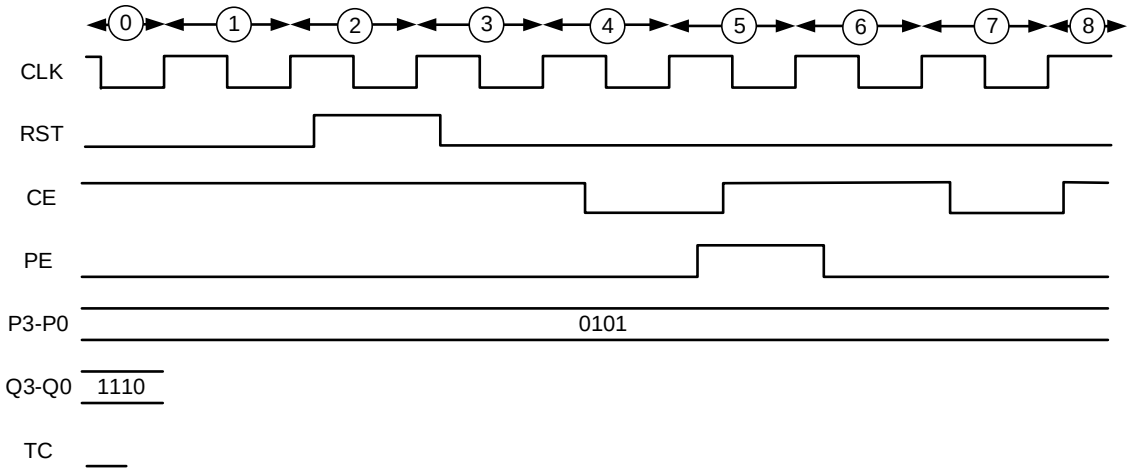
2) [Xilinx] (11 pts.) Build an equivalent full-adder using two half-adders as building blocks along with a **minimal** number of additional gate(s) if needed.

3) [Xilinx] (15 pts.) Using half-adders and full-adders design a circuit that takes in a 5-bit unsigned number, X ($X_4..X_0$) and produces an output equal to X + 21_{10}. Your design should **minimize** the area required (i.e. use half-adders where possible.)

4) [Xilinx] (15 pts.) Design a circuit that takes in four 4-bit unsigned numbers, A ($A_3..A_0$), B ($B_3..B_0$), C ($C_3..C_0$), and D ($D_3..D_0$) and produces the 6-bit unsigned sum of those numbers. You should use **three** 4-bit adder blocks (74LS283's), and a **minimal** number of full adders or half adders. You should organize your adder circuits to perform as many additions in parallel (at the same time) as possible. Getting started: Write out the columns of addition and see where you can apply 4-bit adders. Use half and full adders for remaining addition operations.

HW 4c Blackboard Form (43 pts.)

5) [BB] (25 pts.) Complete the waveform for a synchronous 4-bit counter (positive edge-triggered with active-hi parallel load enable [PE] and count enable [CE]) Q[3:0] and TC outputs that was discussed in class.



6) [BB] (18 pts.) Complete the waveform for a positive-edge triggered, 4-bit D-Register with active-hi data (load) enable and active-low asynchronous reset.

Enter **unk** if the value of Q is unknown during a clock cycle.