EE 209 Homework 1

Redekopp

Name: ___Solutions_____

Due: **Score: _____**

Show work to get full credit. Remember, use on only one side of the paper and staple them together. Only use a calculator to CHECK your work, not to DO your work.

1.a F = (A'+B')(C)

ABC	A'	B'	A' + B'	C	F
000	1	1	1	0	0
001	1	1	1	1	1
010	1	0	1	0	0
011	1	0	1	1	1
100	0	1	1	0	0
101	0	1	1	1	1
110	0	0	0	0	0
111	0	0	0	1	0

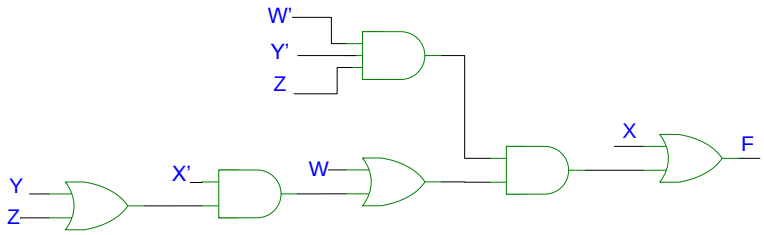
F = A'B'C + A'BC + AB'C
= m1 + m3 + m5
= $\Sigma_{ABC}(1,3,5)$

1.b G = WX' + XY' + W'

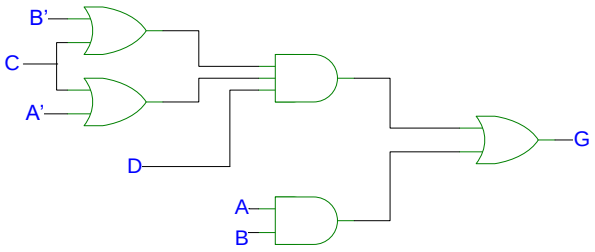
WXY	X'	W • X'	Y'	X • Y'	W'	F
000	1	0	1	0	1	1
001	1	0	0	0	1	1
010	0	0	1	1	1	1
011	0	0	0	0	1	1
100	1	1	1	0	0	1
101	1	1	0	0	0	1
110	0	0	1	1	0	1
111	0	0	0	0	0	0

G = W'+X'+Y'
= M7
= $\Pi_{WXY}(7)$

2.a F = X + (W'Y'Z)(W + (X'(Y + Z)))



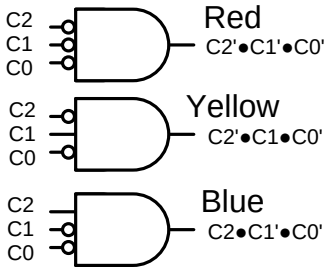
2.b G = AB + D(B' + C)(A' + C)



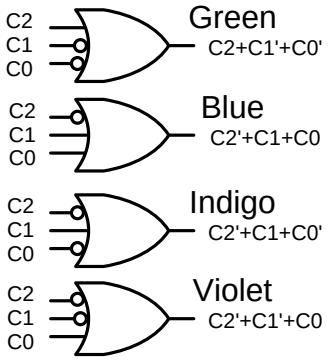
1. **[BB]** (14 pts.) Implement the following functions

	Color Bit Combinations		
Meaning	**C2**	**C1**	**C0**
Red	0	0	0
Orange	0	0	1
Yellow	0	1	0
Green	0	1	1
Blue	1	0	0
Indigo	1	0	1
Violet	1	1	0
Unused	1	1	1

a. Build appropriate single gate (+ inverters) checker/decoders that outputs a logic '1' for each of the three primary colors: **Red, Blue, Yellow** (i.e. one decoder to check for each color)

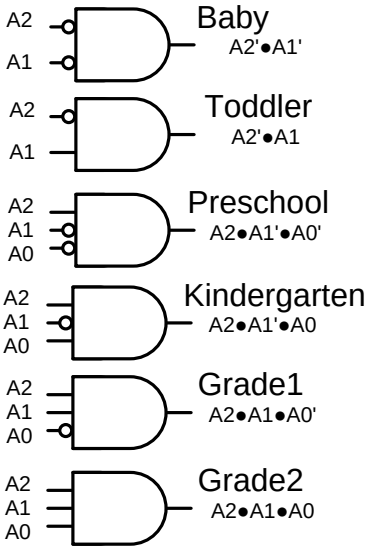


b. Build an appropriate single gate (+inverters) checker/decoder that outputs a logic '0' for each color: **Green, Blue, Indigo, Violet**.



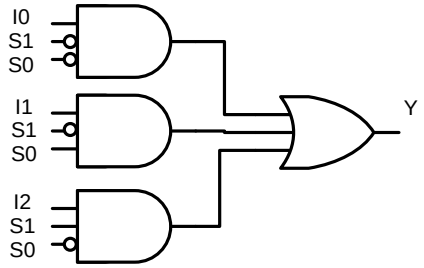
2. **[BB]** (12 pts.) Given a child's age [0-7 years old], design logic to produce the following outputs: {**Baby, Toddler, Preschool, Kinder, Grade1, Grade2**} which have the following age correspondence/mapping. Use only 1 AND gate (and any number of inverters) per output.

	Age Combinations		
Meaning	**A2**	**A1**	**A0**
Baby	0	0	0
	0	0	1
Toddler	0	1	0
	0	1	1
Preschool	1	0	0
Kindergarten	1	0	1
Grade1	1	1	0
Grade2	1	1	1



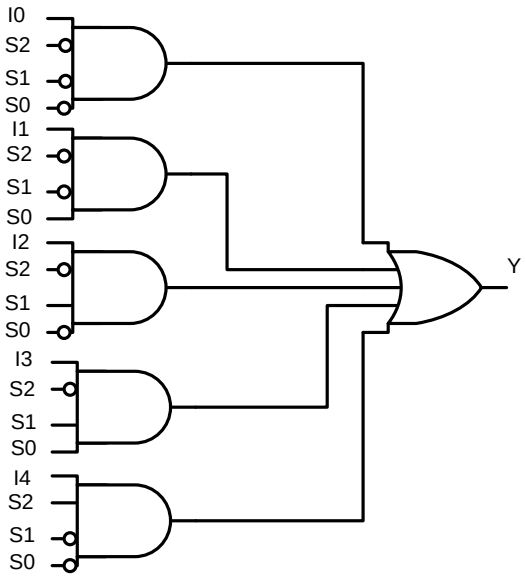
3. **[BB]** (5 pts.) Draw a gate-level schematic of a 3-to-1 mux [Inputs: I0, I1, I2, and select bits S1,S0 and output Y] with the following function table:

S1	S0	Y
0	0	I0
0	1	I1
1	0	I2
1	1	unused



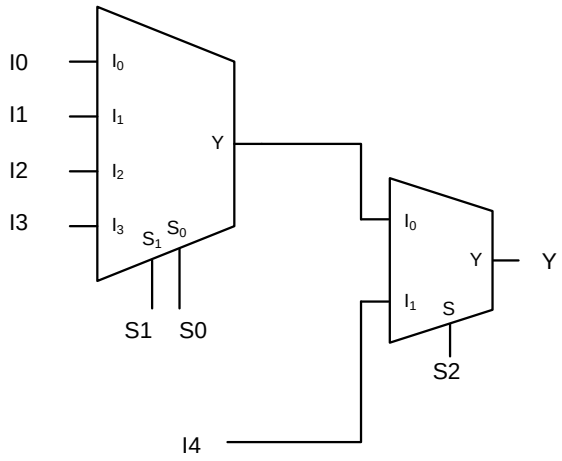
4. **[BB]** (5 pts.) Draw a gate-level schematic of a 5-to-1 mux [Inputs: I0, I1, I2, I3, I4 and select bits S2,S1,S0 and output Y] with the following function table:

S2	S1	S0	Y
0	0	0	I0
0	0	1	I1
0	1	0	I2
0	1	1	I3
1	0	0	I4



5. **[BB]** Could you design the same 5-to-1 mux if we provided a single 4-to-1 mux and a single 2-to-1 mux. If so, show your design.

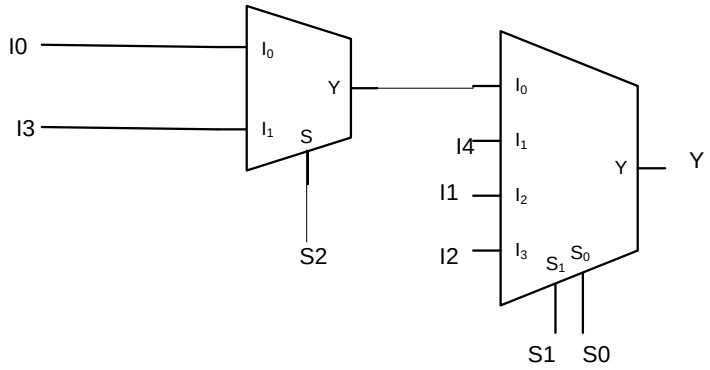
Yes.



6. **[BB]** Suppose we change the select bit correspondence of the 5-to-1 mux from the previous problem to now be as shown in the table below. Could you design a 5-to-1 mux with a single 4-to-1 mux and single 2-to-1 mux. If so, show your design.

S2	S1	S0	Y
0	0	0	I0
0	1	0	I1
0	1	1	I2
1	0	0	I3
1	0	1	I4

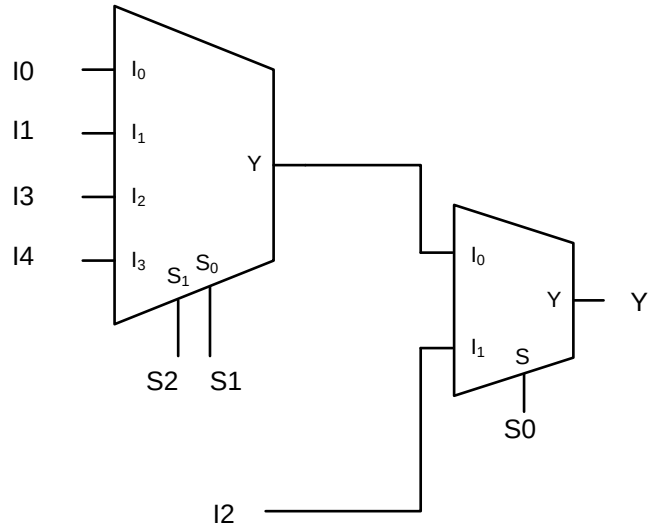
A possible solution:



7. **[BB]** Suppose we change the select bit correspondence of the 5-to-1 mux from the previous problem to now be as shown in the table below. Could you design a 5-to-1 mux with a single 4-to-1 mux and single 2-to-1 mux. If so, show your design.

S2	S1	S0	Y
0	0	0	I0
0	1	0	I1
0	1	1	I2
1	0	0	I3
1	1	0	I4

Yes



8. **[BB]** Given the 5-to-1 mux description in the prior problem (problem 7) and select bit correspondence, draw a gate-level schematic of this circuit.