

EE 209 Homework 1

Fundamental Components

Name: _____

Due: See Website

Score: _____

Please post any questions regarding HW problems on Piazza.

HW 1a Blackboard Form – Answer on Blackboard

- [BB] (16 pts.)** Derive the truth table for the following functions [One basic approach is to simply plug in each combination and evaluate the expression].
 - $F = (A' + B')(C)$
 - $G = WX' + XY' + W'$
- [BB] (14 pts.)** Implement the following functions

Meaning	Color Bit Combinations		
	C2	C1	C0
Red	0	0	0
Orange	0	0	1
Yellow	0	1	0
Green	0	1	1
Blue	1	0	0
Indigo	1	0	1
Violet	1	1	0
Unused	1	1	1

- Build appropriate single gate (+ inverters) checker/decoders that outputs a logic '1' for each of the three primary colors: **Red, Blue, Yellow** (i.e. one decoder to check for each color)
- Build an appropriate single gate (+inverters) checker/decoder that outputs a logic '0' for each color: **Green, Blue, Indigo, Violet**.

3. **[BB] (12 pts.)** Given a child's age [0-7 years old], design logic to produce the following outputs: {**Baby, Toddler, Preschool, Kinder, Grade1, Grade2**} which have the following age correspondence/mapping. Use only 1 AND gate (and any number of inverters) per output.

Meaning	Age Combinations		
	A2	A1	A0
Baby	0	0	0
	0	0	1
Toddler	0	1	0
	0	1	1
Preschool	1	0	0
Kindergarten	1	0	1
Grade1	1	1	0
Grade2	1	1	1

HW 1b – Submit on Paper

4. **[Paper] (8 pts.)** Draw a schematic representation using logic gates (AND, OR, NOT) for the following Boolean equations (use bubbles at the inputs or outputs of AND and OR gates rather than drawing individual inverters)
- $F = X + ((W'Y'Z)(W + (X'(Y+Z))))$
 - $G = AB + (D(B'+C)(A'+C))$
5. **[Paper] (8 pts.)** Draw a gate-level schematic of a 3-to-1 mux [Inputs: I0, I1, I2, and select bits S1, S0 and output Y] with the following function table:

S1	S0	Y
0	0	I0
0	1	I1
1	0	I2
1	1	Unused

6. **[Paper] (10 pts.)** Draw a gate-level schematic of a 5-to-1 mux [Inputs: I0, I1, I2, I3, I4 and select bits S2, S1, S0 and output Y] with the following function table:

S2	S1	S0	Y
0	0	0	I0
0	0	1	I1
0	1	0	I2
0	1	1	I3
1	0	0	I4
others			unused

7. **[Paper] (8 pts.)** Could you design the same 5-to-1 mux if we provided a single 4-to-1 mux and a single 2-to-1 mux. If so, show your design.

8. **[Paper] (6 pts.)** Suppose we change the select bit correspondence of the 5-to-1 mux from the previous problem to now be as shown in the table below. Could you design a 5-to-1 mux with a single 4-to-1 mux and single 2-to-1 mux. If so, show your design.

S2	S1	S0	Y
0	0	0	I0
0	1	0	I1
0	1	1	I2
1	0	0	I3
1	0	1	I4
	others		unused

9. **[Paper] (6 pts.)** Suppose we change the select bit correspondence of the 5-to-1 mux from the previous problem to now be as shown in the table below. Could you design a 5-to-1 mux with a single 4-to-1 mux and single 2-to-1 mux. If so, show your design.

S2	S1	S0	Y
0	0	0	I0
0	1	0	I1
0	1	1	I2
1	0	0	I3
1	1	0	I4
	others		unused

10. **[Paper] (12 pts.)** Given the 5-to-1 mux description in the prior problem (problem 9) and select bit correspondence, draw a gate-level schematic of this circuit.ⁱ

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