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CS356 Unit 15

Review

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Final Jeopardy

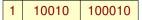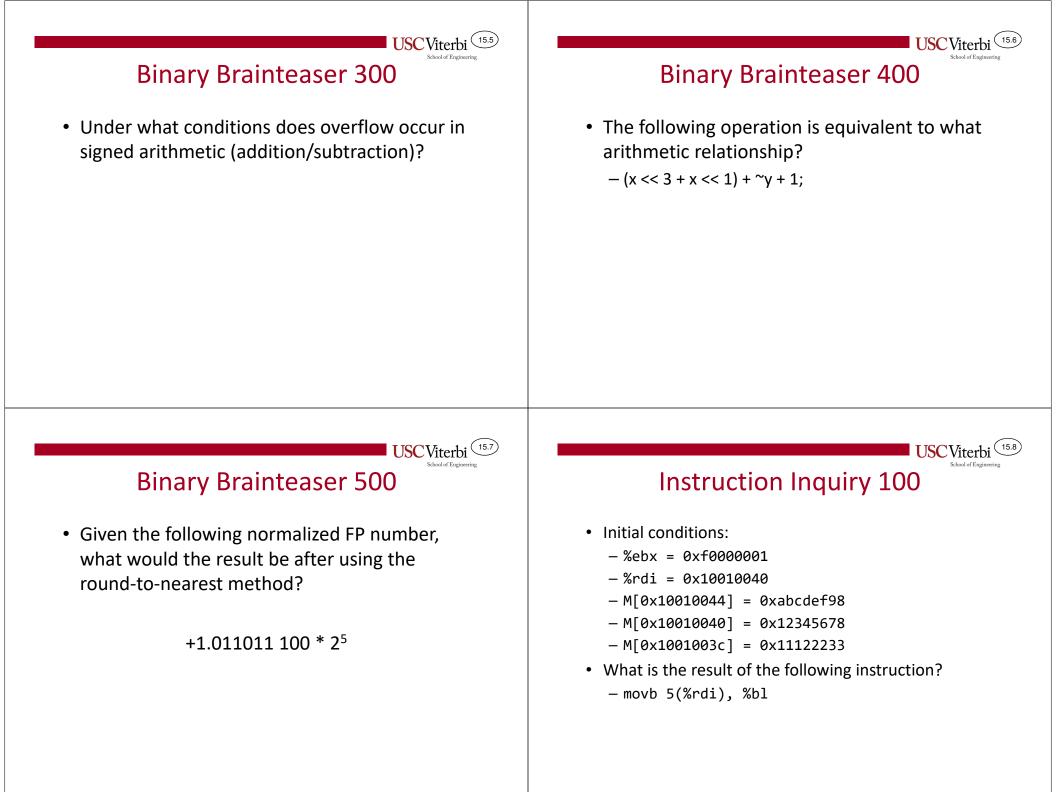| Binary Brainteasers	Instruction Inquiry	Random Riddles	Memory Madness	Processor Predicaments	Programming Pickles
100	100	100	100	100	100
200	200	200	200	200	200
300	300	300	300	300	300
400	400	400	400	400	400
500	500	500	500	500	500

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Binary Brainteaser 100

- Given the binary string "10001101", what would its decimal equivalent be assuming a 2's complement representation?
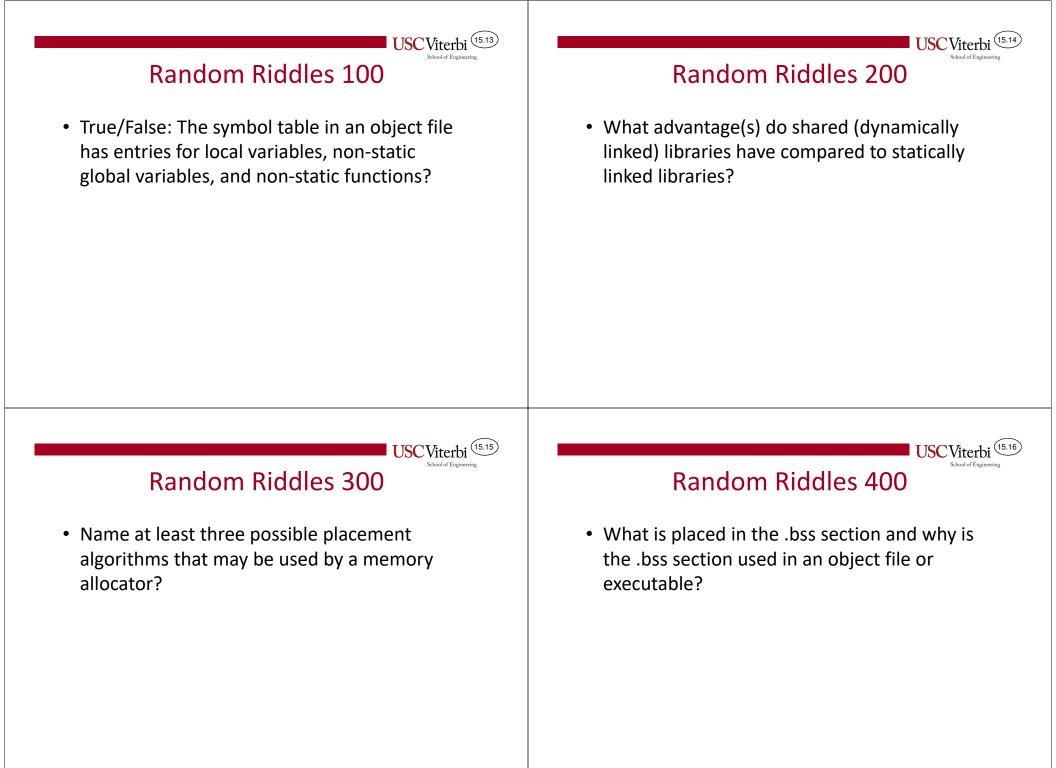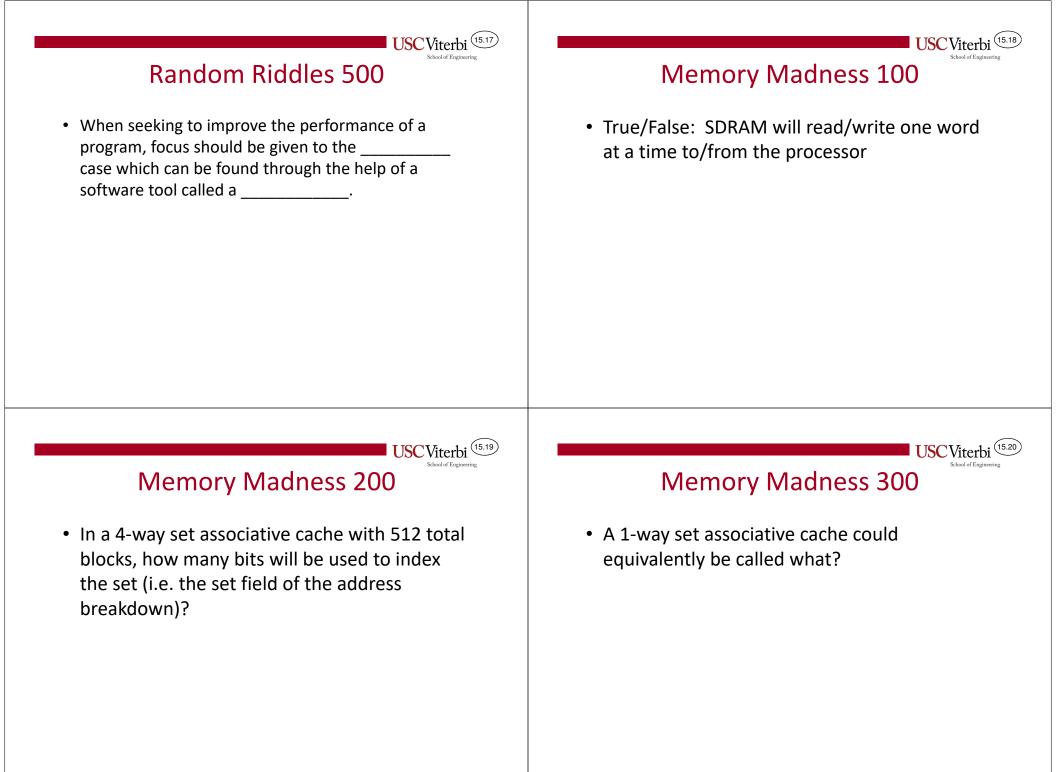

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Binary Brainteaser 200

- Assuming the 12-bit IEEE shortened FP format, what is the decimal equivalent of the following number?

1	10010	100010

Binary Brainteaser 300

- Under what conditions does overflow occur in signed arithmetic (addition/subtraction)?

Binary Brainteaser 400

- The following operation is equivalent to what arithmetic relationship?
  - (x << 3 + x << 1) + ~y + 1;

Binary Brainteaser 500

- Given the following normalized FP number, what would the result be after using the round-to-nearest method?

$$+1.011011\ 100 * 2^5$$

Instruction Inquiry 100

- Initial conditions:
  - %ebx = 0xf0000001
  - %rdi = 0x10010040
  - M[0x10010044] = 0xabcdef98
  - M[0x10010040] = 0x12345678
  - M[0x1001003c] = 0x11122233
- What is the result of the following instruction?
  - movb 5(%rdi), %bl

Instruction Inquiry 200

- Initial conditions:
  - %rbx = 0xffff_ffff_ffff_ffff
  - %rdi = 0x10010040
  - %eax = 0x12345678
  - M[0x10010044] = 0xabcdef34
  - M[0x10010040] = 0x12345678
  - M[0x1001003c] = 0x11122288
- What is the result of the following instruction?
  - movsbw (%rdi,%rbx,4),%eax

Instruction Inquiry 300

- Initial conditions:
  - %ebx = 0xf000000f
- What is the result of the following instruction?
  - xorl %ebx,%ebx

Instruction Inquiry 400

- Initial conditions:
  - %eax = 0x80010000
- What is the result of the following instruction?
  - sarl 1,%eax

Instruction Inquiry 500

- Initial conditions:
  - %rbx = 0x00000001
  - %rdi = 0x1001003c
  - M[0x10010044] = 0xabcdef98
  - M[0x10010040] = 0x12345678
  - M[0x1001003c] = 0x11122233
- What is the result of the following instruction?
  - leal 6(%rdi,%rbx,2), %eax

Random Riddles 100

- True/False: The symbol table in an object file has entries for local variables, non-static global variables, and non-static functions?

Random Riddles 200

- What advantage(s) do shared (dynamically linked) libraries have compared to statically linked libraries?

Random Riddles 300

- Name at least three possible placement algorithms that may be used by a memory allocator?

Random Riddles 400

- What is placed in the .bss section and why is the .bss section used in an object file or executable?

Random Riddles 500

- When seeking to improve the performance of a program, focus should be given to the _____ case which can be found through the help of a software tool called a _____.

Memory Madness 100

- True/False: SDRAM will read/write one word at a time to/from the processor

Memory Madness 200

- In a 4-way set associative cache with 512 total blocks, how many bits will be used to index the set (i.e. the set field of the address breakdown)?

Memory Madness 300

- A 1-way set associative cache could equivalently be called what?

Memory Madness 400

- The page table is located in the (**TLB / memory**) and has entries for
(**all pages residing in physical memory / all pages**)?

Memory Madness 500

- Assume a 24-bit virtual addresses, 1 KB pages and a fully-associative TLB with 128 entries. Assume page table and TLB entries are 2-bytes. How large would the page table be?

Processor Predicaments 100

- A superscalar processor means that the maximum IPC (instructions per clock cycle) is greater than _____?

Processor Predicaments 200

- A control hazard occurs when we execute what kind of instruction(s)?

Processor Predicaments 300

- Of the three kinds of data hazards (RAW, WAR, WAW) which is the only true dependency?

Processor Predicaments 400

- WAR and WAW hazards prevent us from (**reordering instructions / predicting a branch**) and can be solved through _____?

Processor Predicaments 500

- Statically schedule superscalars rely on _____ to schedule the code to avoid hazards while dynamically scheduled superscalars rely on _____ to schedule the code.

Programming Pickles 100

- A programming technique to expose more parallelism in a loop body to the compiler is known as: _____

Programming Pickles 200

- Calling a subroutine will result in the return address being stored (**in the PC / on the stack**)?

Programming Pickles 300

- The stack frame of a subroutine includes space for three sections of data, what are they?

Programming Pickles 400

- The compiler optimization of reproducing the function code at each location where it is called is known as _____

Programming Pickles 500

- A special value placed on the stack between local variables and return address is known as a _____

Cache Operation Example

- Address Trace
  - R: 0x3c0
  - W: 0x048
  - R: 0x3d4
  - W: 0xb50
- Operations
  - Hit
  - Fetch block XX
  - Evict block XX (w/ or w/o WB)
  - Final WB of block XX)

- Perform address breakdown and apply address trace
- 2-Way Set-Assoc, N=8, B=32 bytes

Address	Tag	Set	Byte Offset
0x3c0			
0x048			
0x3d4			
0xb50			

Processor Access	Cache Operation
R: 0x3c0	
W: 0x048	
R: 0x3d4	
W: 0xb50	
Done!	

2-way VLIW Scheduling

- No forwarding w/in an issue packet (between instructions in a packet)
- Full forwarding paths for instructions already in the pipeline even across slots/pipes (i.e. from 'add' in MEM stage to 'lw' in EX stage)
- Latency of LW is still 1 stall cycle for dependent instructions
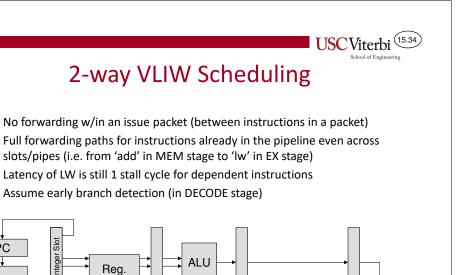- Assume early branch detection (in DECODE stage)

Sample Scheduling

- Schedule the following loop body on our 2-way static issue machine
  - You can modify code and re-arrange but not unroll loops or rename registers

```
for(i=MAX-1; i != 0; i--,A++,B++)
   *A = *A + *B;
```

```
%rdi = pointer to A
%rsi = pointer to B
%edx = i = # of iterations

L1: ld    (%rdi),%eax
    ld    (%rsi),%ebx
    addl %ebx,%eax
    st   %eax,(%rdi)
    addl $4,%rdi
    addl $4,%rsi
    addl $-1,%edx
    jne  $0,%edx,L1
```

Int./Branch Slot	LD/ST Slot

Sample Scheduling

- Now unroll the loop two ways and use register renaming and schedule the code (feel free to modify aspects of the code as needed to ensure better scheduling).

```
%rdi = pointer to A
%rsi = pointer to B
%edx = i = # of iterations

L1: ld    (%rdi),%eax
    ld    (%rsi),%ebx
    addl %ebx,%eax
    st   %eax,(%rdi)
    ld   _____
    ld   _____
    addl _____
    st   _____
    addl ____,%rdi
    addl ____,%rsi
    addl ____,%edx
    jne  $0,%edx,L1
```

Int./Branch Slot	LD/ST Slot